User's Manual

2801630

Version 1.1

Year: 2007

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How to Use This Manual

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The manual describes how to configure your 2801630 system board to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Global American, Inc.** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site :
http://www.globalamericaninc.com./.

Chapter 1
System Overview

1.1 Introduction

Global American, Inc., a world-leading innovator in the Industrial PC (IPC) market, has launched its new 2801630 in response to market demand for a simplified embedded system board (ESB) that combines robust computing power, a smaller footprint and lower power consumption with increased product longevity. The 2801630 Mini-ITX ESB utilizes the latest Intel® Q965 and ICH8DO chipset to support Intel® Core™ 2 Duo and Pentium® 4/Celeron® D processors. Its features include dual display, single GbE LAN port, PCI and mini-PCI expansion slots, four SATA ports, four COM ports, RAID (0,1,5,10) and six USB 2.0 ports in a compact 170 mm x 170 mm (6.69˝ x 6.69˝) form factor that weighs a mere 0.43 kg (0.94 lbs).

Available now, 2801630 Mini-ITX ESB is the ideal solution for applications in medical equipment, storage device control, gaming machines, digital signage, kiosks, semiconductor equipment and automation control equipment.

Intel Q965 GMCH and Watchdog timer

Mini-ITX ESB of 2801630 supports Intel® Core™ 2 Duo and Pentium® 4/Celeron® D processors, adopts Intel® Q965 chipset, includes GPIO and Watchdog timer.

1.2 Check List

The 2801630 package should cover the following basic items

- One 2801630 Mini ITX Main Board
- Two Serial ATA cable
- One Serial port cable for COM2
- One I/O Shield bracket
- One Installation Resources CD-Title

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**
  - Support Intel Core 2 Duo and Pentium 4 processor / Celeron D processor
  - CPU bus clock: 1066/800/533 MHz
- **Chipset**
  Intel® Q965 GMCH & ICH8DO
- **Main Memory**
  - Support dual-channel & signal channel DDR memory interface
  - Up to 4GB DDR2 800 SDRAM on two 240pin DIMM sockets
- **System BIOS**
  AWARD BIOS
- **Expansion Interface**
  One PCI expansion slot, and support up to two PCI slots by riser card
- **SATA Interface**
  Four SATA ports
- **Serial Ports**
  Support four serial ports, (RS-232x4)

- **IR Interface**
  N/A
- **Parallel Port**
  N/A
- **USB Interface**
  Support six USB (Universal Serial Bus) ports (two at rear, four on-board for internal devices)
- **PS/2 Mouse and Keyboard Interface**
  Support dual 6-pin mini-DIN connector at rear I/O panel for PS/2 keyboard/mouse
- **Audio Interface**
  Connector of Line-in/Line-out/MIC
- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar
- **Watchdog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - Generate system reset
- **On-board VGA**
  - Intel Q965 GMCH Integrated GMA 3000 Graphics device
  - Intel DVMT 4.0 supports up to 384MB video memory
- **On-board Ethernet LAN**
  Gigabit Ethernet (10/100/ 1000 Mbits/sec) LAN port
- **High Driving GPIO**
  Onboard programmable 8-bit Digital I/O interface
- **Cooling Fans**
  Support one 4-pin power connector for CPU cooler and one 3-pin power connector for system fan
- **System Monitoring Feature**
  Monitor system temperature and major power sources, etc
- **Outline Dimension (L X W):**
  170mm (6.69″) X 170mm (6.69″)

- **Power Requirements:**
- **Configuration:**

  CPU: Intel Core 2 Dou 2.13GHz (FSB:1066 / 2MB)

  Memory: Transcend DDR2 533 1GB (SEC K4T51083QC)

  VGA: Onboard Intel 83566DM

  Audio: Onboard Realtek ALC260

  SCSI Card: Adaptec AHA-2940

  SCSI HDD: Seagate ST318453LW

  CDROM: Plextor PX-755SA

  PSU: PW-330ATXE-12V

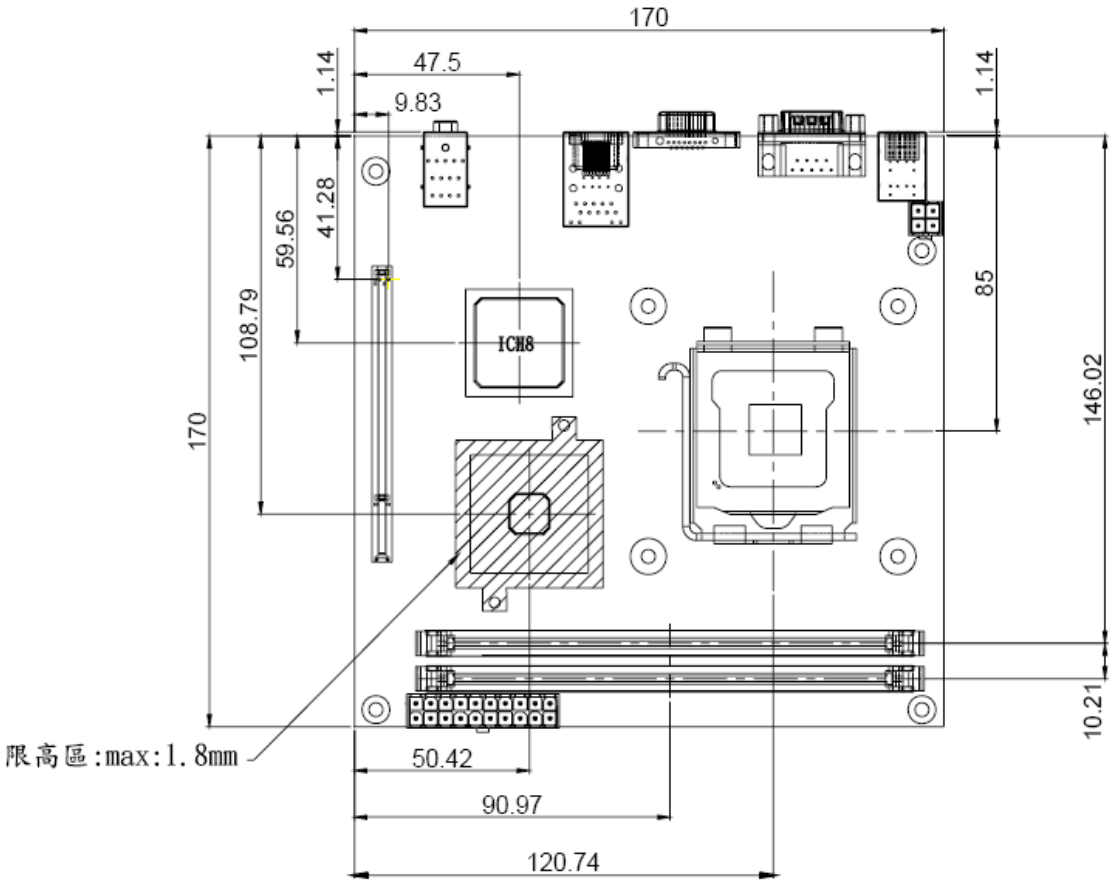
  Run Burning Test V4.0.

  RUN time: 10 / 30 Minutes.

Item	Power ON	Full Loading 10Min	Full Loading 30Min
CPU +12V	2.77	2.57	2.52
System +12V	0.62	0.53	0.51
System +3.3V	2.35	0.3	0.25
System +5V	5.1	4.72	4.7

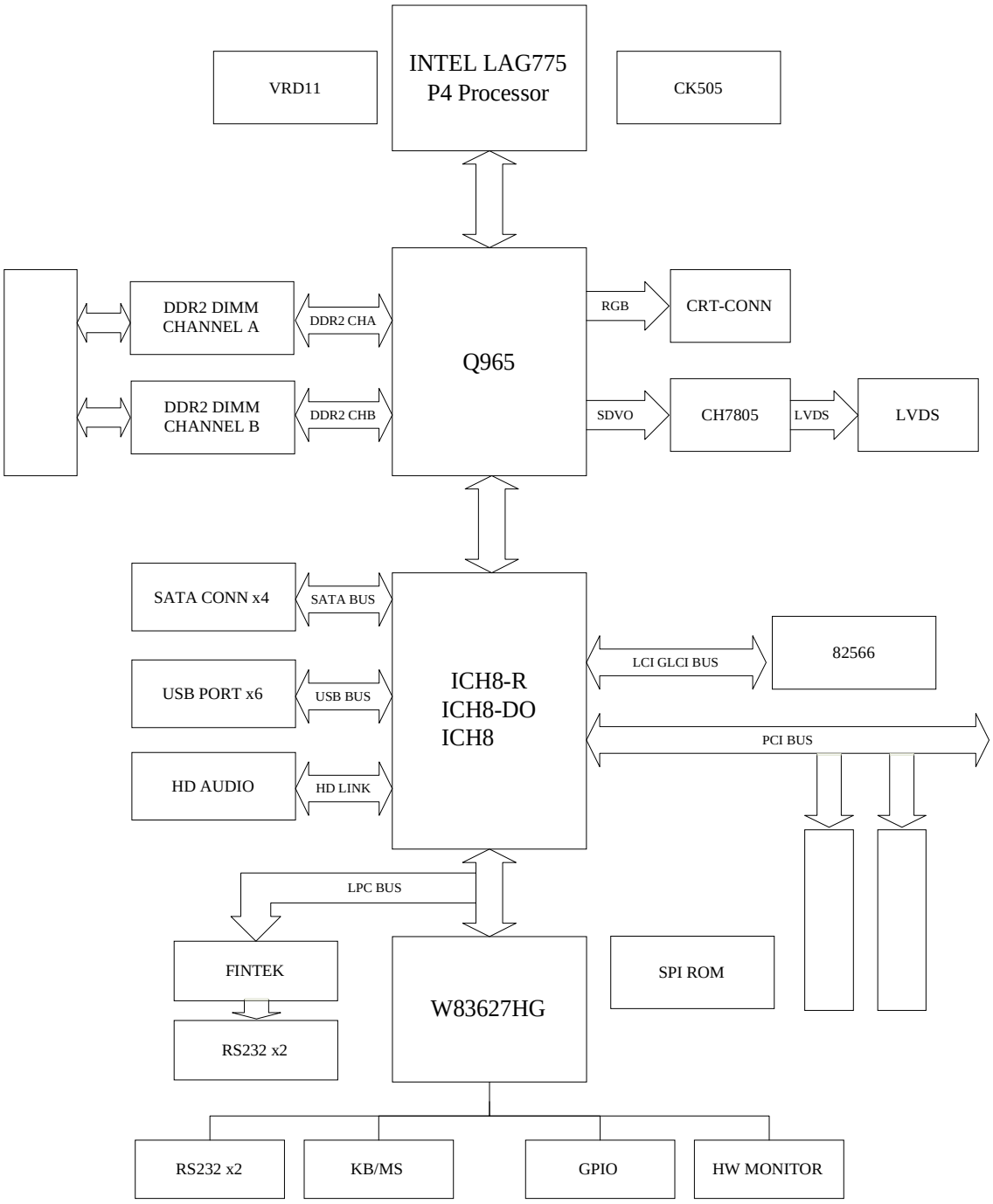
- **Operating Temperature:**
  0°C ~ 55°C
- **Storage Temperature:**
  -20°C ~ 80°C
- **Relative Humidity:**
  5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



1.4 System Architecture

All of details operating relations are shown in 2801630 series System Block Diagram.



2801630 System Block Diagram

Chapter 2
Hardware Configuration

This chapter indicates jumpers', headers' and connectors' locations. Users may find useful information related to hardware settings in this chapter. The default settings are indicated with a star sign (✚).

2.1 Jumper Setting

For users to customize 2801630's features. In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper locations.

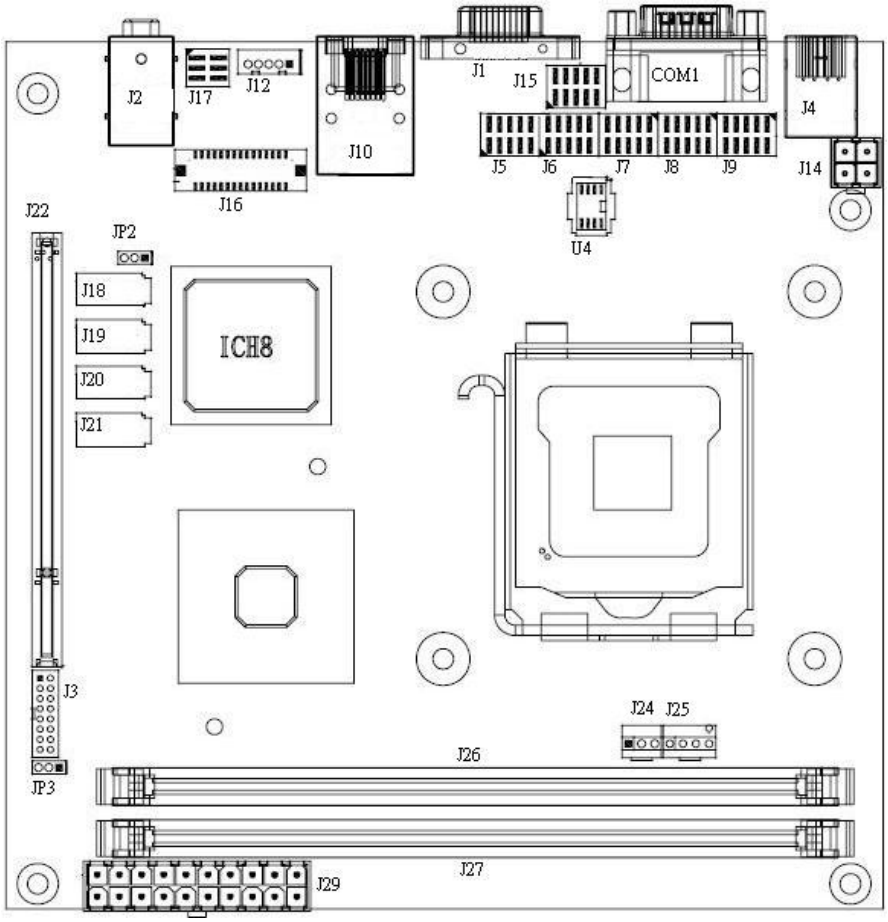


Figure 2-1 2801630 Jumper and Connector Locations

JP2: VDDLVDS_IN Selection

JP2	Function
1-2 Short	VCC3 ✚
2-3 Short	VCC

Note :
Wrong voltage selection may damage the LVDS panel.
Please survey LVDS panel's VDD before setup this jumper setting.

JP3: CMOS Clear

JP3	Function
1-2 Short	Normal Operation ✚
2-3 Short	Clear CMOS Contents

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

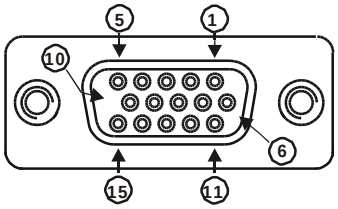
Connector Function List

Connector	Function	Remark
J1	VGA CONNECTOR	
J2	AUDIO CONNECTOR	
J3	Power/LED Header	
J4	PS2/KB&MS	
J5, J6	USB CONNECTOR	
J7	COM3 CONNECTOR	
J8	COM4 CONNECTOR	
J9	COM2 CONNECTOR	
J10	GLAN+USBx2 CONNECTOR	
J12	BACK LIGHT POWER connector	
J14	CPU PWR CONN	
J15	8-bit GPIO	
J16	LVDS connector	
J17	LVDS VDD SETTING	
J18, J19, J20, J21	SATA CONNECTOR	
J22	PCI SLOT	
J24	SYSTEM Fan connector	
J25	CPU Fan connector	
J26, J27	DDRII SOCKET	

J29	PWR CONN	
J30	Mini-PCI	
BT1	VBAT CONNECTOR	
COM1	COM1 CONNECTOR	

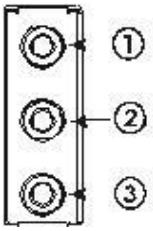
Pin Assignments of Connectors

J1: VGA Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	RED	2	GREEN
3	BLUE	4	ID0
5	Ground	6	Ground
7	Ground	8	Ground
9	NC	10	Ground
11	ID1	12	DDCDATA
13	HSYNC	14	VSYNC
15	DDCCLK		

J2: Audio Jack Connector



PIN No.	Signal Description
1 (Blue)	Line In
2 (Lime)	Line Out
3 (Pink)	Mic In

J3: Power/LED Header

PIN No.	Signal Description		Signal Description
1	Speaker Signal	2	POWER_LED+ (5V)
3	NC	4	NC
5	NC	6	POWER_LED-
7	+5V	8	KEYLOCK
9	PWRBTN	10	Ground
11	PWRBTN	12	NC
13	RESET	14	HDD_LED+ 5V (1K ohm)
15	RESET	16	HDD_LED-

J5 & J6: USB CONNECTOR

	Signal Description	PIN No.	Signal Description
1	USB power (5V)	2	USB power (5V)
3	USB DATA A-	4	USB DATA B-
5	USB DATA A+	6	USB DATA B+
7	GND	8	GND
9	N/C	10	N/C

J12: BACK LIGHT POWER connector

Pin No.	Signal Description
1	ENABLE
2	GND
3	+12V
4	GND
5	VCC

Note :
Wrong voltage selection may damage the LVDS panel's back light inverter.
Please survey inverter's maximum allow input level before setup this jumper setting.

J15: 8-bit GPIO

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO10	2	GPIO11
3	GPIO12	4	GPIO13
5	Ground	6	GPIO14
7	GPIO15	8	GPIO16
9	GPIO17	10	5V

J16: LVDS connector

1	LCD1DO0+	2	LCD1DO0-
3	LCD1DO1+	4	LCD1DO1-
5	LCD1DO2+	6	LCD1DO2-
7	LCD1DO3+	8	LCD1DO3-
9	LCD1CLK+	10	LCD1CLK-
11	LCD2DO0+	12	LCD2DO0-
13	LCD2DO1+	14	LCD2DO1-
15	LCD2DO2+	16	LCD2DO2-
17	LCD2DO3+	18	LCD2DO3-
19	LCD2CLK+		LCD2CLK-
21	LDATA1	22	LCLK1
23	GND	24	N/C
25	GND	26	Ground
27	POWER	28	POWER
29	N/C	30	POWER

J17: LVDS VDD SETTING

Pin No.	Signal Description
1-3, 2-4	5V, Active High
1-3, 4-6	12V, Active High
3-5,2-4	5V, Active Low
3-5,4-6	12V, Active Low

J24: SYSTEM Fan connector

Pin No.	Signal Description
1	PWM_CONTROL
2	+12V
3	SENSE

J25: CPU Fan connector

Pin No.	Signal Description
1	GND
2	+12V
3	SENSE
4	PWM_CONTROL

COM1 & J9 & J7 & J8: COM PORT connector

Pin No.	Signal Description
1	Data Carrier Detect
2	Receive Data
3	Transmit Data
4	Data Terminal Ready
5	Ground
6	Data Set Ready
7	Request To Send
8	Clear To Send
9	Ring Indicator
10	N/C

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® LGA 775 Processor

Installing LGA775 CPU

1) Lift the handling lever of CPU socket outwards and upwards to the other end. Following step A position to step B position.

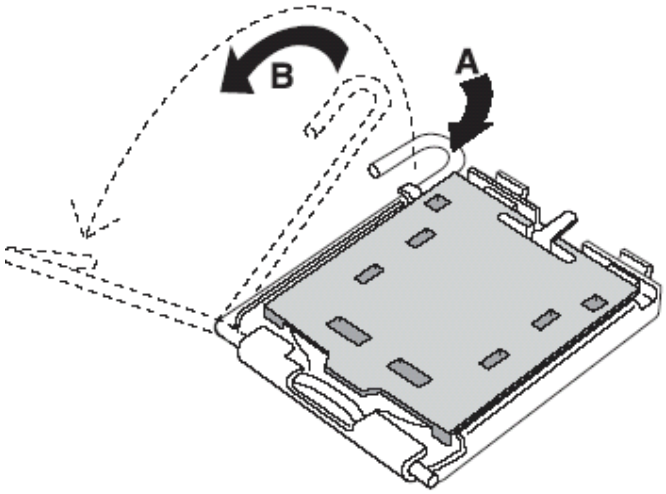


Figure 3-1

2) Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place (see Fig.3-4). If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.

Triangle mark is meaning first pin position; kindly assemble and take aim at notch of top and bottom between CPU and socket.

Figure 3-2

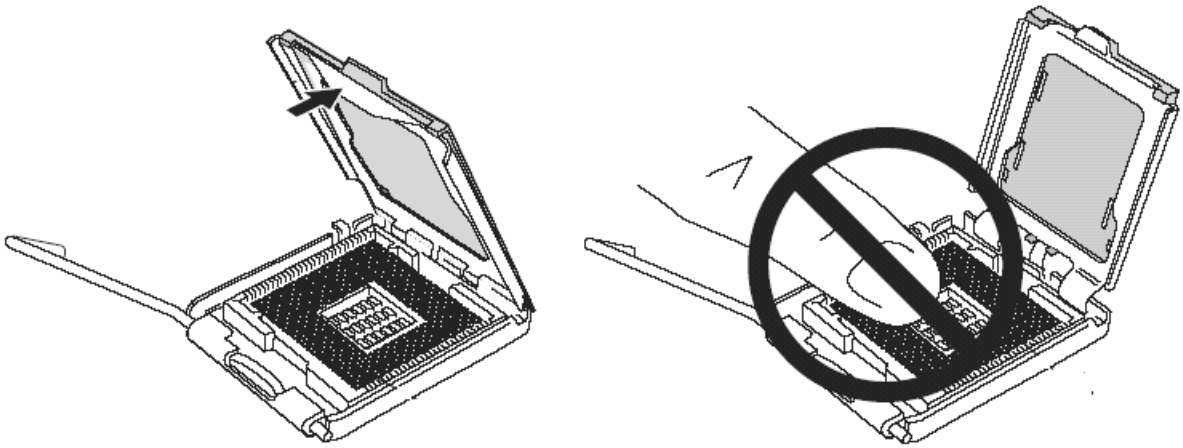


Figure 3-3

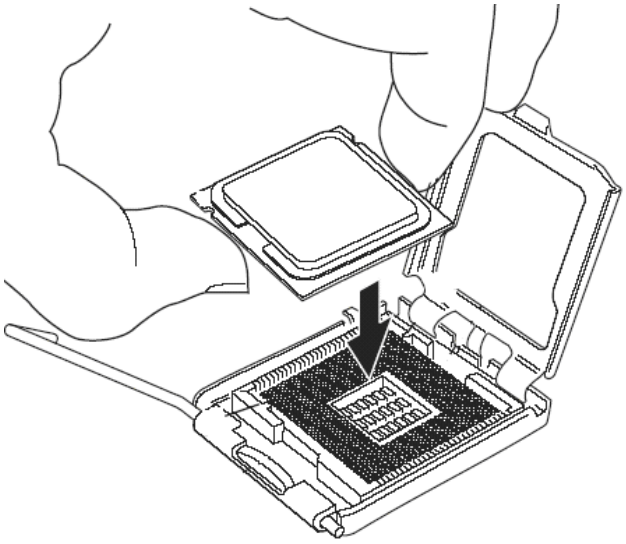


Figure 3-4

Precaution! (See fig.3-3) Don't touch directly by your hand or impacts internal align balls of CPU socket to avoid motherboard destruction, it is a precise actuator.

3) Push down the lever to lock processor chip into the socket once CPU fits.

4) Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the LGA 775.

Removing CPU

1) Unlock the cooling fan first.
2) Lift the lever of CPU socket outwards and upwards to the other end.
3) Carefully lifts up the existing CPU to remove it from the socket.
4) Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

Configuring System Bus

2801630 will automatically detect the CPU used. CPU speed of Intel P4 /Celeron D can be detected automatically.

3.2 Main Memory

2801630 provides Two DIMM sockets which supports 800/667/533 DDR2-SDRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory size can be up to 4GB capacity. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or two single-sided DIMM in both sockets.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Dual Channel DDR DIMMs

Supporting dual-channel & signal channel DDR2 memory technology, adequate for higher bandwidth of memory than processor would increase system performance. To enable Dual Channel DDR2 memory technology, install two identical memory modules in both memory sockets is required. Following tables show bandwidth information of different processor and memory configurations.

Following tables have not thing to do with the Dual Channel DDR2 DIMMs, may be cancel them or have new topic.

CPU FSB	Bandwidth
1066MHz	8.5GB/s
800MHz	6.4GB/s
533MHz	4.2GB/s

	Dual Channel DDR Bandwidth	Single Channel DDR Bandwidth
800MHz	6.4 GB/s	3.2 GB/s
677MHz	5.4 GB/s	2.7 GB/s
533 MHz	4.2 GB/s	2.1 GB/s

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

Memory frequency / CPU FSB synchronization

2801630 supports different memory frequencies depending on the CPU front side bus and the type of DDR2 DIMM.

CPU FSB	Memory Frequency
1066MHz	800/667/533MHz
800MHz	667/533MHz
533 MHz	533MHz

3.3 Installing the Single Board Computer

To install your 2801630 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place 2801630 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.3.2 Chipset Component Driver

The chipset used on 2801630 is relatively new which operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows-2000/XP, please install its INF before any of other Drivers are installed.

3.3.3 Intel Integrated Graphics GMCH Chip

Using Intel® Q965 GMCH with Media Accelerator (GMA) 3000 High performance graphic integrated chipset is aimed to gain an outstanding graphic performance. It is accompanied by shared up to 384MB video memory with Intel DVMT 4.0. This combination makes 2801630 an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI VGA card can take over the system display.

Drivers Support

Please find Springdale GMC driver in the 2801630 CD-title. Drivers support Windows-2000, Windows XP and Linux.

3.3.4 Gigabit Ethernet Controller

Drivers Support

Please find Intel 825660M LAN driver in /Ethernet directory of 2801630 CD-title. The drivers support Windows-2000 and Windows-XP.

LED Indicator (for LAN status)

2801630 provides two LED indicators to report Intel 825660M Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">825660M</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><th colspan="2">ON</th><th>OFF</th></tr>
<tr><td>Status LED</td><td>Green</td><td>LAN Linked & Active LED</td><td colspan="2">Linked</td><td>Active (Blinking)</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">LAN speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.3.5 Audio Controller

Please find Realtek ALC260 Audio driver form 2801630 CD-title. The drivers support Windows 2000 and XP.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP3	Function
1-2 Short	Normal Operation ✚
2-3 Short	Clear CMOS contents

To correctly operate CMOS Clear function, user must turn off the system, move JP3 jumper to short pin 2 and 3. To clear CMOS contents, please turn the power back on and turn it off again for AT system, or press the toggle switch a few times for ATX system. Move the JP3 back to 1-2 position (Normal Operation) and start the system. System will then produce a "CMOS Check Sum Error" message and hold up. Users may then follow the displayed message to load BIOS default setting.

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

2801630 allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to Winbond W83627HG-AW data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
//Step1. Enter W83627HG configuration registers mode:
outportb(0x2E, 0x87);
outportb(0x2E, 0x87);

//* Step2. Pin89 to be WDTO
outportb(0x2E, 0x2b);
outportb(0x2E + 1, 0x04);

//* Step3. Select logic device 8:
outportb(0x2E, 0x07);
outportb(0x2E + 1, 0x08);

//* Step4. Config WDT using second to be unit:
outportb(0x2E, 0xf5);
outportb(0x2E + 1, 0x00);

//* Step5. Set WDT time-out time:
outportb(0x2E, 0xf6);
outportb(0x2E + 1, time_out);

//* Step6. Exit configuration registers mode:
outportb(0x2E, 0xaa);
```

3.6 GPIO

The 2801630 provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.6.1 Pin assignment

J15: General Purpose I/O Connector

PIN No.	Signal Description
1	General Purpose I/O Port 0 (GPIO0)
2	General Purpose I/O Port 1 (GPIO1)
3	General Purpose I/O Port 2 (GPIO2)
4	General Purpose I/O Port 3 (GPIO3)
5	Ground
6	General Purpose I/O Port 4 (GPIO4)
7	General Purpose I/O Port 5 (GPIO5)
8	General Purpose I/O Port 6 (GPIO6)
9	General Purpose I/O Port 7 (GPIO7)
10	+5V

All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each source sink capacity up to 12mA.

3.6.2 2801630 GPIO Programming Guide

There are 8 GPIO pins on 2801630. These GPIO pins are from SUPER I/O (W83627GH-AW) GPIO pins, and can be programmed as Input or Output direction.

J15 pin header is for 8 GPIO pins and its pin assignment as following :

J15_Pin1=GPIO0:from SUPER I/O_GPIO10 with Ext. 4.7K PH
J15_Pin2=GPIO1:from SUPER I/O_GPIO11 with Ext. 4.7K PH
J15_Pin3=GPIO2:from SUPER I/O_GPIO12 with Ext. 4.7K PH
J15_Pin4=GPIO3:from SUPER I/O_GPIO13 with Ext. 4.7K PH
J15_Pin6=GPIO4:from SUPER I/O_GPIO14 with Ext. 4.7K PH
J15_Pin7=GPIO5:from SUPER I/O_GPIO15 with Ext. 4.7K PH
J15_Pin8=GPIO6:from SUPER I/O_GPIO16 with Ext. 4.7K PH
J15_Pin9=GPIO7:from SUPER I/O_GPIO17 with Ext. 4.7K PH

<<<<< Be careful Pin5=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of W83627HG-AW needed to be programmed to control the GPIO direction, and status(GPI)/value(GPO). CR00h ~ CR2F are common (global) registers to all Logical Devices (LD) in W83627HG. CR07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO10~17 registers.

Programming Guide:

Step1: CR2A_Bit [7.2]. P [1,1,1,1,1,1]; to select multiplexed pins as GPIO10~17 pins
Step2: LD7_CR07h.P [07h]; Point to LD7
Step3: LD7_CR30h_Bit0.P1; Enable LD7
Step4: Select GPIO direction, Get Status or output value.

LD7_CRF0h; GPIO17 ~ 10 direction, 1 = input, 0 = output pin
LD7_CRF2h.P [00h]; Let CRF1 (GPIO data port) non-invert to prevent from confusion
LD7_CRF1h; GPIO17~10 data port, for input pin, get status from the related bit, for output pin, write value to the related bit.

For example,

LD7_CRF0h_Bit4.P0; Let GPIO14 as output pin
LD7_CRF2h_Bit4.P0; Let CRF1_Bit4 non-inverted
LD7_CRF1h_Bit4.P0; Output "0" to GPIO14 pin (J25_Pin6)

LD7_CRF0h_Bit0.P1; Let GPIO10 as input pin
LD7_CRF2h_Bit0.P0; Let CRF1_Bit0 non-inverted
Read LD7_CRF1h_Bit0; Read the status from GPIO10 pin (J25_Pin1)

How to access W83627HG CR?

In 2801630, the EFER = 002Eh, and EFDR = 002Fh.
EFER and EFDR are 2 IO ports needed to access W83627HG-AW CR.
EFER is the Index Port, EFDR is the Data Port.
CR index number needs to be written into EFER first,
Then the data will be read/written from/to EFDR.

To R/W W83627HG-AW CR, it is needed to Enter/Enable Configuration Mode first. When completing the programming, it is suggested to Exit/Disable Configuration Mode.

Enter Configuration Mode: Write 87h to IO port EFER twice.
Exit Configuration Mode: Write AAh to IO port EFER.

3.6.3 Example

```
void enter_Superio2_CFG(void)
{
   outportb(0x2E, 0x87);
   outportb(0x2E, 0x87);
}


void exit_Superio2_CFG(void)
{
   outportb(0x2E, 0xAA);
}


void Set_CFG2(unsigned char Addr2,unsigned char Value2)
{
  unsigned char d2;
   outportb(0x2E, Addr2);
   delay(2);
   outportb(0x2E +1, Value2);
   delay(2);
}


unsigned char Get_CFG2(unsigned char Addr2)
{
  unsigned char d2;
   outportb(0x2E, Addr2);
   delay(2);
   d2 = inportb(0x2E +1);
   delay(2);
   return(d2);
}

int main(void)
{

   unsigned char d2;
```

```
   enter_Superio2_CFG();
   /* CR2A B7 = 1 selet GPIO Port 1*/
   d2 = Get_CFG2(0x2A);
   d2 = (d2 & 0x7F) | 0x80;
   Set_CFG2(0x2A, d2);

   /* IO test loop 1 */
   /* Set GPIO Port 1 of Superio 2 Enable */

   Set_CFG2(0x07, 0x07);    /* Select logic device 07 of Superio2*/
   Set_CFG2(0x30, 0x01);    /* Enable GPIO Port 1 of Superio2*/



   /* IO test loop 1 */

   /* Set GPIO Port 1 of Superio2 Enable */
   Set_CFG2(0x07, 0x07);    /* Select logic device 07*/
   Set_CFG2(0xF0, 0x0F);      /* GPIO Port 1 of Superio2 is [ooooiiii], o: output, i:input
*/
   Set_CFG2(0xF2, 0x00);      /* GPIO Port 1 of Superio2 is non-inversed*/



   Set_CFG2(0x07, 0x07);    /* Select logic device 07*/
   Set_CFG2(0xF1, 0xFF);    /* Initial back all GPIO Port1 of Superio 2 to hi */

   Set_CFG2(0x07, 0x07);    /* Select logic device 07*/
   Set_CFG2(0xF1, 0xEF);    /* GP14 of Superio2 -> ~GP10 of Superio2 */
   Set_CFG2(0x07, 0x07);    /* Select logic device 07 of Superio2*/
   d2 = Get_CFG2(0xF1);     /* get GPIO Port 2 data */

   if (d2 == 0xEE )

     printf("\n GPIO14->10 test ok");
   else
     printf("\n GPIO14->10 test fail ");
```

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Device Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0483	16K	DOS
0484-053F	2.9K	Program Area
0540-9EFE	614K	Available
9EFF-9EFF	0.1K	Unused
= Conventional memory ends at 640K =		
9F00-9FBF	3K	Extended Bios Area
9FC0-9FFF	1K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CAFF	44K	Video ROM
CB00-CC49	5.2K	Unused
CC4A-DFFF	78K	High RAM
E000-EFFF	60K	Unused
EF00-EFFF	4K	ROM
F000-FFFF	64K	System ROM
HMA	64K	First 64K Extended

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	Unassigned	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	Unassigned	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unassigned	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	Unassigned	Usable IRQ
IRQ 10	Unassigned	Usable IRQ
IRQ 11	Unassigned	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	Unassigned	Usable IRQ

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support you for your products, projects and business.

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