integration with integrity

2808010 User's Manual

Mini-ITX Mainboard

Version 1.0

Safety Instructions

1. Always read the safety instructions carefully.
2. Keep this User's Manual for future reference.
3. Keep this equipment away from humidity.
4. Lay this equipment on a reliable flat surface before setting it up.
5. The openings on the enclosure are for air convection hence protects the equipment from overheating. DO NOT COVER THE OPENINGS.
6. Make sure the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
7. Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
8. Always Unplug the Power Cord before inserting any add-on card or module.
9. All cautions and warnings on the equipment should be noted.
10. Never pour any liquid into the opening that could damage or cause electrical shock.
11. If any of the following situations arises, get the equipment checked by service personnel:
    - † The power cord or plug is damaged.
    - † Liquid has penetrated into the equipment.
    - † The equipment has been exposed to moisture.
    - † The equipment does not work well or you can not get it work according to User's Manual.
    - † The equipment has dropped and damaged.
    - † The equipment has obvious sign of breakage.
12. DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT UNCONDITIONED, STORAGE TEMPERATURE ABOVE 60°C (140°F), IT MAY DAMAGE THE EQUIPMENT.

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.

警告使用者:
這是甲類的資訊產品，在居住的環境中使用時，可能會造成無線電干擾，在這種情況下，使用者會被要求採取某些適當的對策。

廢電池請回收

For better environmental protection, waste batteries should be collected separately for recycling or special disposal.

FCC-B Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the measures listed below.

- † Reorient or relocate the receiving antenna.
- † Increase the separation between the equipment and receiver.
- † Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- † Consult the dealer or an experienced radio/television technician for help.

Notice 1
The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2
Shielded interface cables and A.C. power cord, if any, must be used in order to comply with the emission limits.

VOIR LA NOTICE D'INSTALLATION AVANT DE RACCORDER AU RESEAU.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and
(2) this device must accept any interference received, including interference that may cause undesired operation.

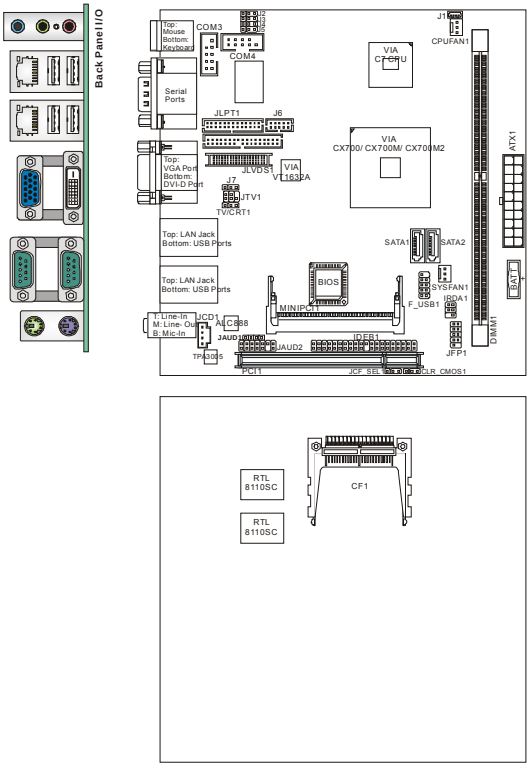
CONTENTS

Chapter 1
Product Overview

Thank you for choosing the Fuzzy 2808010 Mini ITX mainboard from GAI.

Noiseless, fanless and low power consumption are the advantages of the Fuzzy CX700/CX700D, making it an ideal choice for IPC special application.

Mainboard Layout



2808010 Mini ITX Mainboard

Chapter 2
Product Specifications

Based on the innovative VIA CX700/ CX700M/ CX700M2 controller for optimal system efficiency, the Fuzzy CX700/CX700D accommodates VIA C7/ Eden/ Eden ULV processor and supports one 240-pin 400/533MHz DDR2 DIMM slot to provide the maximum of 1GB memory capacity.

Mainboard Specifications

Processor Support

- VIA C7/ Eden/ Eden ULV processor with nanoBGA2 footprint
- 3-pin CPU fan pinheader with Smart Fan Speed Control
- Power Saver™ Technology enabled

CPU Frequency

- 1GHz, 1.5GHz, or 2GHz (Optional)
- Supports FSB to 400/800MHz (Optional)

Chipset

- Single chip solution: VIA CX700/ CX700M/ CX700M2

Memory Support

- DDR2 400/533 SDRAM or ECC DDR2 400 only (1GB Max)
- 1 DDR2 DIMM slot (240pin / 1.8V)

LAN

- 2 PCI Gb LAN by Realtek RTL8110SC

Audio

- Realtek ALC888 7.1-channel HDA codec
- 6 watt amplifier

IDE

- 1 40-pin IDE connector
- Supports 2 IDE devices

CF

- 1 CF Type II socket

SATA

- 2 SATA II ports by VIA CX700/ CX700M/ CX700M2
- Supports storage and data transfers at up to 300MB/s

Expansion Slots

- 1 PCI slot
- 1 Mini PCI socket

Connectors

- **Rear I/O**
  - 1 PS/2 mouse port
  - 1 PS/2 keyboard port
  - 1 COM port stack connector (2 RS-232 ports)
  - 1 VGA/ DVI stack connector
  - 2 RJ45/ USB stack connectors
  - 1 3-jack audio connector

- **Onboard Connector**
  - 1 USB connector (2 ports)
  - 1 parallel port connector (LPT)
  - 2 COM port connectors (RS-232)
  - 1 LVDS connector
  - 1 DIO connector (4 IN/ 4 OUT)
  - 1 TV-Out connector
  - 1 audio connector (7.1-channel)
  - 1 amplifier connector
  - 1 front panel connector
  - 1 SMBUS connector
  - 1 CPU fan connector
  - 1 system fan connector
  - 2 SATA connectors

Form Factor

- Mini-ITX (17.0cm X17.0cm)

Mounting

- 4 mounting holes

Environmental

- **Operating Temperature**
  - Temperature: 0°C ~ 60°C
  - Humidity: 0% ~ 85% RH

- **Storage Temperature**
  - Temperature: -20°C ~ 80°C
  - Humidity: 25% ~ 90% RH

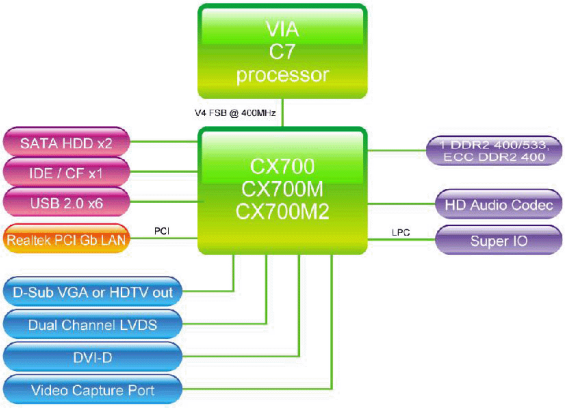
Safety Compliance & MTBF

Certification	Standard number		Title of standard
CE	RFI	EN 55022:1998+A1:2000+A2:2003 Class B	Product family standard
		EN 6100-3-2:2000 Class D	Limits for harmonic current emission
		EN 6100-3-3:1995+A1:2001	Limitation of voltage fluctuation and flicker in low-voltage supply system
	Immunity	EN 55024:1998+A1:2001+A2:2003	Product family standard
BSMI	CNS 13438 乙類(1997年版)		
C-Tick	AS/NZS CISPR 22:2004		
FCC	FCC CFR Title 47 Part 15 Subpart B: 2005 Class B		
	CISPR 22: 2005		
VCCI	VCCI V-3:2004, Class B		
	VCCI V-4:2004, Class B		

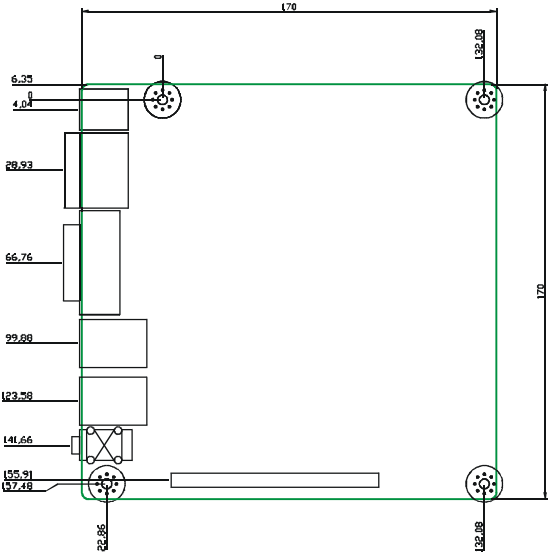
MTBF - Reliability Prediction

Calculation Model	Operation Temperature	Operating Environment	Duty Cycle	MTBF
Telcordia Issue 1	35	Ground Benign	100%	186,718
MIL-HDBK-217 FN2	55	Ground Mobile	100%	3,182

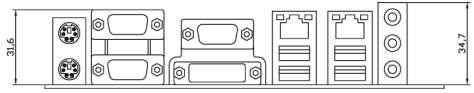
Block Diagram

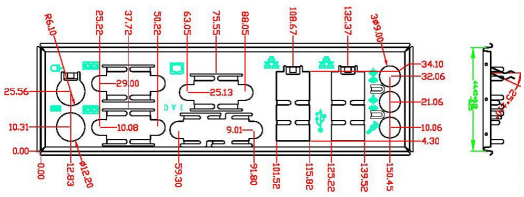


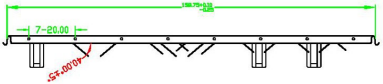
Board Dimension



I/O Shield Drawing







Chapter 3
Electrical Specifications

This chapter provides detailed electrical specifications of this mainboard. For safety concern, users are advised to read this chapter first before powering on the mainboard.

Power Consumption

Configuration
CPU：VIA C7 1GHz
Memory：Samsung PC2-3200 1GB
SATA HDD：HITACHI 80GB
SATA HDD：Maxtor 80GB
CDROM：Samsung CD-RW/DVD

Power Consumption					
	Mainboard +3.3V	Mainboard +5V	Mainboard 5VSB	Mainboard +12V	System Consumption
	Current (A)	Current (A)	Current (A)	Current (A)	Watts
A. Full Running (CPU / Memory / HDD / LAN stress & Play Audio CD)	1.33	1.07	0.04	0.67	18.0773
B. Running Network Application - Files Copy	1.33	1.04	0.039	0.6	17.0905
C. Idle	0.56	0.94	0.04	0.39	11.482
D. S3 Mode	0	0	0.318	0	1.6345
E. Running 3D stress	1.972	6.2115	0.1748	7.709	16.0673

General Purpose I/O Lines

General Purpose I/O Lines			
Parameter	Conditions	Min	Max
Input High Voltage (VIH)	-	2V	2V
Input High Voltage (VIL)	-	-0.5V	0.8V
Input Current (II)	-	-	+(-)1uA
Out High Voltage (VoH)	IOH = -50uA	4.4V	-
	IOH = -16uA	3.8V	-
Out Low Voltage (VoL)	IOL = 50uA	-	0.1V
	IOH = 16uA	-	0.55V

Onboard Connector

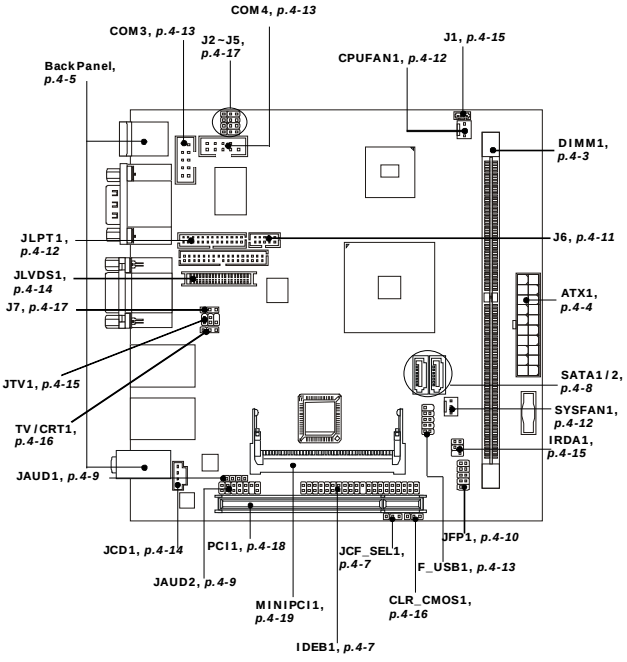
Onboard Connector		Description
DC 12V power connector		2x2-pin, 4.2mm
AMP audio header		1x4-pin, 2.54mm
GPIO box header		2x5-pin, 2mm
Parallel port box header		2x13-pin, 2mm
LVDS panel box header		2x20pin, 1.25mm
RS-232 box header (internal)		2x5pin, 2.54mm (take out of 1-pin)
TV-OUT header		2x3-pin, 2.54mm (take out of 1-pin)
Front panel I/O header		2x5-pin, 2.54mm (take out of 1-pin)
IrDA header		2x3-pin, 2.54mm (take out of 1-pin)
USB header (internal)		2x5-pin, 2.54mm (take out of 1-pin)
Front audio header		2x7-pin, 2.54mm (take out of 1-pin)

Chapter 4
Hardware Setup

This chapter provides you with the information about hardware setup procedures. While doing the installation, be careful in holding the components and follow the installation procedures. For some components, if you install in the wrong orientation, the components will not work properly.

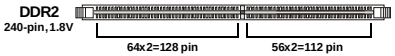
Use a grounded wrist strap before handling computer components. Static electricity may damage the components.

Quick Components Guide



Memory

The mainboard provides one 240-pin **non-ECC DDR2 400/533** and **ECC DDR2 400** DIMM slot and supports up to 1GB system memory.



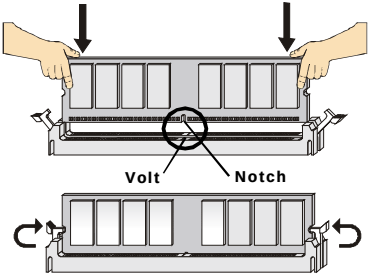
Installing DDR2 Modules

1. The memory module has only one notch on the center and will only fit in the right orientation.
2. Insert the memory module vertically into the DIMM slot. Then push it in until the golden finger on the memory module is deeply inserted in the DIMM slot.

Important

You can barely see the golden finger if the memory module is properly inserted in the DIMM slot.

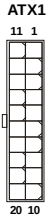
3. The plastic clip at each side of the DIMM slot will automatically close.



Power Supply

ATX 20-Pin System Power Connector: ATX1

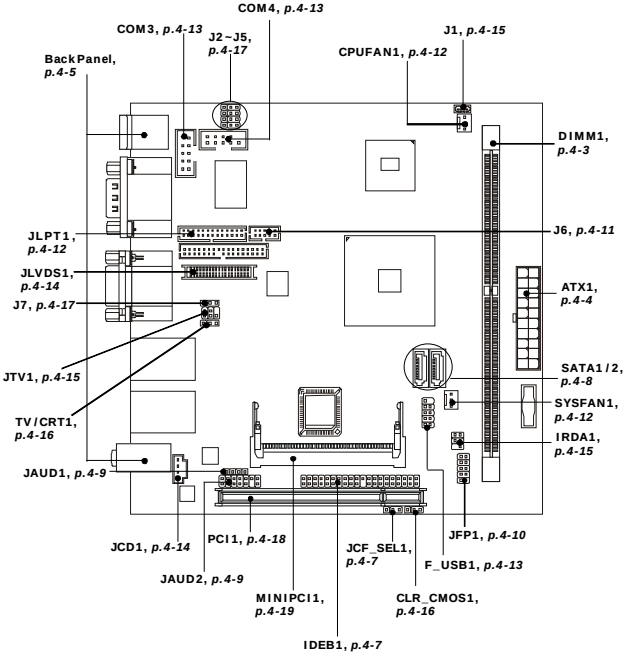
This connector allows you to connect to an ATX power supply. To connect to the ATX power supply, make sure the plug of the power supply is inserted in the proper orientation and the pins are aligned. Then push down the power supply firmly into the connector.



ATX1 Pin Definition

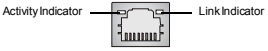
PIN	SIGNAL	PIN	SIGNAL
1	3.3V	11	3.3V
2	3.3V	12	-12V
3	GND	13	GND
4	5V	14	PS_ON
5	GND	15	GND
6	5V	16	GND
7	GND	17	GND
8	PW_OK	18	-5V
9	5V_SB	19	5V
10	12V	20	5V

Quick Components Guide



▶ LAN (RJ-45) Jacks

The standard RJ-45 jacks are for connection to Local Area Network (LAN). You can connect network cables to them.



		Left LED	Right LED
		Active LED	**100M/1000M Speed LED**
LED Color		Yellow	Green/Orange
10M Cable Plug-in	**No Transmission**	OFF	OFF
	Transition	Yellow(Blinking)	OFF
100M Cable Plug-in	**No Transmission**	OFF	Green(Lighting)
	Transition	Yellow(Blinking)	Green(Lighting)
1000M Cable Plug-in	**No Transmission**	OFF	Orange(Lighting)
	Transition	Yellow(Blinking)	Orange(Lighting)
In S3/S4/S5 Standby State		OFF	OFF

Connectors

IDE Connector: IDEB1

The mainboard has a 32-bit Enhanced PCI IDE and Ultra DMA 33/66/100/133 controller that provides PIO mode 0~4, Bus Master, and Ultra DMA 33/66/100/133 function. You can connect hard disk drives, CD-ROM and other IDE devices.

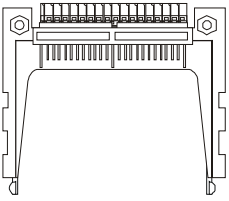
The Ultra ATA133 interface boosts data transfer rates between the computer and the hard drive up to 133 megabytes (MB) per second.

IDEB1

CompactFlash Card Slot: CF1

This CompactFlash slot shares one channel of the IDE controller. You can install one CompactFlash typel / type II device.

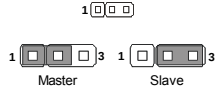
CF1



CF Mode Selecting Jumper: JCF_SEL1

This jumper is used to select Master/ Slave mode of the CF device.

JCF_SEL1

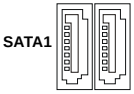


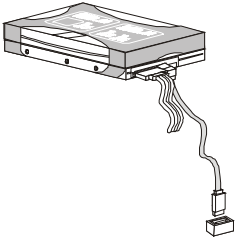
Important

* *The CF1 slot and the IDEB1 connector shares and uses the same channel. CF1 and IDEB1 can support up to 2 IDE devices without CF device or 1 IDE device with 1 CF device.*
* *If you install two IDE devices, you must configure the second drive to Slave mode by setting its jumper. Refer to the hard disk documentation supplied by hard disk vendors for jumper setting instructions.*
* *If you install one IDE device with ATA133 IDE cable and one CF device, you must configure the CF drive to Master mode by setting jumper JCF_SEL1. CF only supports Master mode by using the ATA133 IDE cable.*
* *CF only supports Slave mode by using ATA33 IDE cable.*

Serial ATA Connectors: SATA1, SATA2

SATA1~SATA2 are high-speed SATA interface ports and support SATA data rates of 300MB/s. Each SATA connector can connect to 1 hard disk device and is fully compliant with Serial ATA 2.0 specifications.





Important

Please do not fold the Serial ATA cable into 90-degree angle. Otherwise, data loss may occur during transmission.

Audio Amplifier Connector: JAUD1

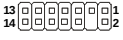
The 6W JAUD1 is used to connect audio amplifiers to enhance audio performance.

Pin Definition

PIN	SIGNAL
1	AMP_R+
2	AMP_R-
3	AMP_L+
4	AMP_L-

Front Audio Connector: JAUD2

This connector is designed to connect an optional audio bracket that provides extra front panel audio IO jacks.



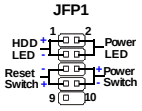
Audio Bracket
(Optional)

JAUD2 Pin Definition

PIN	SIGNAL	PIN	SIGNAL
1	5V_SB	2	VCC3
3	SPDF_OUT	4	NA
5	GND	6	SPDF_IN
7	LEF_OUT	8	SURR_OUT_R
9	CEN_OUT	10	SURR_OUT_L
11	JAUD_DET	12	AUDIO GND
13	SIDE_SURR_L	14	SIDE_SURR_R

Front Panel Connector: JFP1

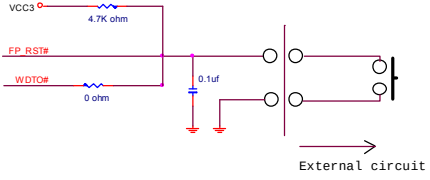
The mainboard provides one front panel connector for electrical connection to the front panel switches and LEDs. The JFP1 is compliant with Intel® Front Panel I/O Connectivity Design Guide.



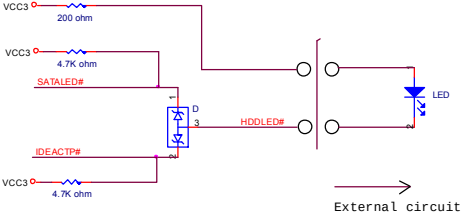
JFP1 Pin Definition

PIN	SIGNAL	DESCRIPTION
1	HD_LED +	Hard disk LED pull-up
2	FPPWR/SLP	MSG LED pull-up
3	HD_LED -	Hard disk active LED
4	FPPWR/SLP	MSG LED pull-up
5	RST_SW-	Reset Switch low reference pull-down to GND
6	PWR_SW+	Power Switch high reference pull-up
7	RST_SW+	Reset Switch high reference pull-up
8	PWR_SW-	Power Switch low reference pull-down to GND
9	RSVD_DNU	Reserved. Do not use.

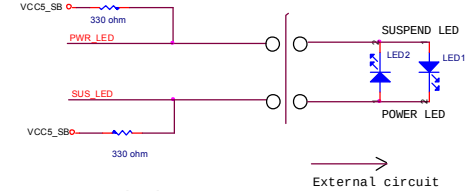
Reset Circuit



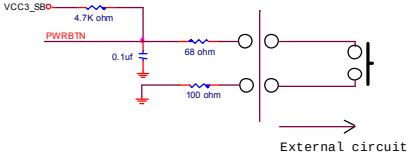
HDD LED Circuit



Power LED Circuit



Power Button Circuit



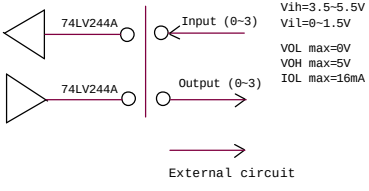
Digital IO Connector: J6

The J6 connects to the General-Purpose Input/Output (GPIO) peripheral module.

J6 Pin Definition

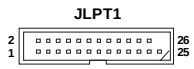
PIN	SIGNAL	PIN	SIGNAL
1	GND	2	VCC5F
3	N_GPO3	4	N_GPO1
5	N_GPO2	6	N_GPO0
7	N_GPI3	8	N_GPI1
9	N_GPI2	10	N_GPI0

DIO Circuit



Parallel Port Header: JLPT1

The mainboard provides a 26-pin header for connection to an optional parallel port bracket. The parallel port is a standard printer port that supports Enhanced Parallel Port (EPP) and Extended Capabilities Parallel Port (ECP) mode.



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	RSTB#	2	AFD#	15	PRND6	16	GND
3	PRND0	4	ERR#	17	PRND7	18	GND
5	PRND1	6	PINIT#	19	ACK#	20	GND
7	PRND2	8	LPT_SLIN#	21	BUSY	22	GND
9	PRND3	10	GND	23	PE	24	GND
11	PRND4	12	GND	25	SLCT	26	GND
13	PRND5	14	GND				

Fan Power Connectors: CPUFAN1, SYSFAN1

The fan power connectors support system cooling fan with +12V. When connecting the wire to the connectors, always take note that the red wire is the positive and should be connected to the +12V, the black wire is Ground and should be connected to GND. If the mainboard has a System Hardware Monitor chipset on-board, you must use a specially designed fan with speed sensor to take advantage of the CPU fan control.

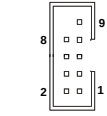
CPUFAN1 SYSFAN1

Important

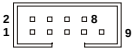
Please refer to the recommended CPU fans at VIA's official website or consult the vendors for proper CPU cooling fan.

Serial Port Connector: COM3, COM4

The mainboard provides two 9-pin headers as serial ports. These ports are 16550A high speed communication port that sends/receives 16 bytes FIFOs. You can attach a serial mouse or other serial devices directly to them.



COM3



COM4

Pin Definition

PIN	SIGNAL	DESCRIPTION
1	DCD	Data Carry Detect
2	SIN	Serial In or Receive Data
3	SOUT	Serial Out or Transmit Data
4	DTR	Data Terminal Ready
5	GND	Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	VCC_COM3	Power Source

Front USB Connector: F_USB1

The mainboard provides one USB 2.0 pinheader that is compliant with Intel® I/O Connectivity Design Guide. USB 2.0 technology increases data transfer rate up to a maximum throughput of 480Mbps, which is 40 times faster than USB 1.1, and is ideal for connecting high-speed USB interface peripherals such as **USB HDD**, **digital cameras**, **MP3 players**, **printers**, **modems and the like**.

F_USB1

Pin Definition

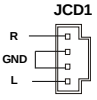
PIN	SIGNAL	PIN	SIGNAL
1	VCC	2	VCC
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	GND	8	GND
9	Key (no pin)	10	USBOC

Important

Note that the pins of VCC and GND must be connected correctly to avoid possible damage.

CD-In Connector: JCD1

The connector is for CD-ROM audio connector.

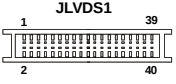


LVDS Flat Panel Connector: JLVDS1

The LVDS (Low Voltage Differential Signal) connector provides a digital interface typically used with flat panels. After connecting an LVDS interfaced flat panel to the JLVDS1, be sure to check the panel datasheet and set the J1 LVDS Power Selection Jumper to a proper voltage.

Display Matrix				
	CRT	DVI	LVDS	TV OUT
CRT		V	V	X
DVI	V		V	V
LVDS	V	V		V
TV OUT	X	V	V	

V : Support X : No Support



SIGNAL	PIN		SIGNAL
+12V	2	1	+12V
+12V	4	3	+12V
GND	6	5	+12V
GND	8	7	VCC3/VCC5
LCD_VDD	10	9	LCD_VDD
LDDC_DATA	12	11	LDDC_CLK
LVDS_VDDEN	14	13	L_BKLTCTL
GND	16	15	L_BKLTEN
LA_DATA0	18	17	LA_DATA0#
LA_DATA1	20	19	LA_DATA1#
LA_DATA2	22	21	LA_DATA2#
LA_CLK	24	23	LA_CLK#
LA_DATA3	26	25	LA_DATA3#
GND	28	27	GND
LB_DATA0	30	29	LB_DATA0#
LB_DATA1	32	31	LB_DATA1#
LB_DATA2	34	33	LB_DATA2#
LB_CLK	36	35	LB_CLK#
LB_DATA3	38	37	LB_DATA3#
GND	40	39	GND

TV-Out Connector: JTV1

The mainboard provides a TV-Out connector.

JTV1

Display Matrix				
	CRT	DVI	LVDS	TV OUT
CRT		V	V	X
DVI	V		V	V
LVDS	V	V		V
TV OUT	X	V	V	

V : Support X : No Support

JTV1 Pin Definition

Pin	Description	Pin	Description
1	TVGND	2	LCVBS
3	LY	4	TVGND
5	LC	6	Key (no pin)

IrDA Infrared Module Header: IRDA1

The connector allows you to connect to IrDA Infrared module. You must configure the setting through the BIOS setup to use the IR function. IRDA1 is compliant with Intel® Front Panel I/O Connectivity Design Guide.

IRDA1

Pin Definition

Pin	Signal
1	NC
2	Key (no pin)
3	VCC5
4	GND
5	IRTX
6	IRRX

I2C Bus Connector: J1

The mainboard provides one I2C (also known as I^2C) Bus connector for users to connect System Management Bus (SMBus) interface.

J1

Pin Definition

Pin	Signal
1	VCC5F
2	SMBCLK
3	GND
4	SMBDATA-

Jumpers

Display Jumper: TV/CRT1

This jumper is used to select the display type.

Display Matrix				
	CRT	DVI	LVDS	TV OUT
CRT		V	V	X
DVI	V		V	V
LVDS	V	V		V
TV OUT	X	V	V	

V : Support X : No Support

Clear CMOS Jumper: CLR_CMOS1

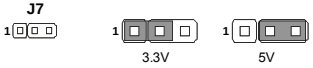
There is a CMOS RAM onboard that has a power supply from external battery to keep the data of system configuration. With the CMOS RAM, the system can automatically boot OS every time it is turned on. If you want to clear the system configuration, set this jumper to clear data.

Important

You can clear CMOS by shorting 2-3 pin while the system is off. Then return to 1-2 pin position. Avoid clearing the CMOS while the system is on; it will damage the mainboard.

LCD Power Source Jumper: J7

This jumper is used to select the power source of LCD.

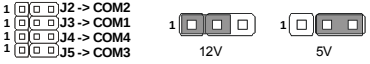


Pin Definition

Pin	Signal
1	VCC3
2	LCD_SRC (default VCC3)
3	VCC5

COM Port Power Jumpers: J2, J3, J4, J5

These jumpers specify the operation voltage of the serial port COM1~4.



Pin Definition

Pin	Signal
1	VCC12F
2	VCC_COM
3	VCC5F

Slots

PCI (Peripheral Component Interconnect) Slot

The PCI slot supports LAN cards, SCSI cards, USB cards, and other add-on cards that comply with PCI specifications. At 32 bits and 33 MHz, it yields a throughput rate of 133 MBps.

32-bit PCI Slot

PCI Interrupt Request Routing

The IRQ, acronym of interrupt request line and pronounced I-R-Q, are hardware lines over which devices can send interrupt signals to the microprocessor. The PCI IRQ pins are typically connected to the PCI bus pins as follows:

	Order 1	Order 2	Order 3	Order 4
32-bit PCI1	INT A#	INT B#	INT C#	INT D#

Important

When adding or removing expansion cards, make sure that you unplug the power supply first. Meanwhile, read the documentation for the expansion card to configure any necessary hardware or software settings for the expansion card, such as jumpers, switches or BIOS configuration.

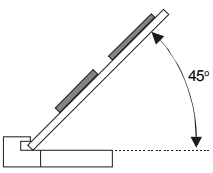
Mini PCI Slot

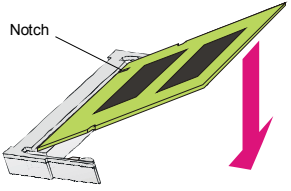
This is a 32 bits, 33 MHz and 133 MBps PCI slot, only select the MiniPCI adapters can be installed.

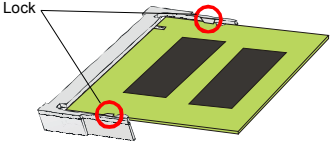
Mini PCI Slot

Installing Mini PCI Cards

1. Insert the card at an angle of 45 degrees into the Mini PCI slot, Line up the notch in the card with the small tab in the slot and slide the card into the slot until the golden finger is almost invisible.
2. Push the Mini PCI card down until the two snaps on either side of the card lock into place.

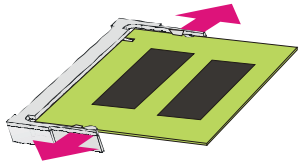


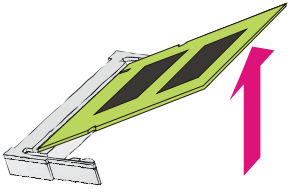




Removing Mini PCI Cards

If you need to remove a card in the Mini PCI slot, spread the tabs in the slot away from the notches in the card. The card should pop up slightly. Lift the card to a 45-degree angle and then gently slide the card out of the slot.





Slots

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32-bit PCI Slot

PCI Interrupt Request Routing

The IRQ, acronym of interrupt request line and pronounced I-R-Q, are hardware lines over which devices can send interrupt signals to the microprocessor. The PCI IRQ pins are typically connected to the PCI bus pins as follows:

	Order 1	Order 2	Order 3	Order 4
32-bit PCI1	INT A#	INT B#	INT C#	INT D#

Important

When adding or removing expansion cards, make sure that you unplug the power supply first. Meanwhile, read the documentation for the expansion card to configure any necessary hardware or software settings for the expansion card, such as jumpers, switches or BIOS configuration.

Chapter 6
System Resources

This chapter provides information on the following system resources:

Watch Dog Timer Setting

Logical Device 7 (Game Port and GPIO Port 1)

CRF3 (PLED mode register. Default 0x00)

Bit [7:3] : Reserved .

Bit 2: select WDTO count mode.

0 second

1 minute

Bit [1:0]: select PLED mode

00 Power LED pin is tri-stated.

01 Power LED pin is droved low.

10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.

11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit [7:0]: = 0x00 Time-out Disable

= 0x01 Time-out occurs after 1 second/minute

= 0x02 Time-out occurs after 2 second/minutes

= 0x03 Time-out occurs after 3 second/minutes

.....

= 0xFF Time-out occurs after 255 second/minutes

CRF5 (Default 0x00)

Bit [7] : Reserved .

Bit [6] : invert Watch Dog Timer Status

Bit 5: Force Watch Dog Timer Time-out, Write only*

1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

1 Watch Dog Timer time-out occurred.

0 Watch Dog Timer counting

Bit [3:0]: These bits select IRQ resource for Watch Dog. Setting of 2 selects S

MI.

Software code

```
SIO_IDX    equ   4EH
SIO_DTA    equ   4FH
Timer      equ   10          ;reset after 10 seconds
1.    Enter configuration mode
      mov  dx,SIO_IDX
      mov  al,87h
      out   dx,al
      out   dx,al

2     Set Pin118 to WDTO#
      mov  dx,SIO_IDX
      mov  al,2Bh
      out   dx,al
      mov  dx,SIO_DTA
      in    al,dx
      and  al,not 04h
      out   dx,al

3.    Set to and active LDN 08
      mov  dx,SIO_IDX
      mov  al,07h
      out   dx,al
      mov  dx,SIO_DTA
      mov  al,08h
      out   dx,al

      mov  dx,SIO_IDX
      mov  al,30h
      out   dx,al
      mov  dx,SIO_DTA
      in    al,dx
      or    al,01h
      out   dx,al

4.    Set WatchDog Timer
      mov  dx,SIO_IDX
      mov  al,0f4h
      out   dx,al
      mov  dx,SIO_DTA
      mov  al,Timer
      out   dx,al

5.    Exit configuration mode
      mov  dx,SIO_IDX
      mov  al,0AAh
      out   dx,al
```

Award POST Code

Award BIOS Error Message and Check Point (POST code) List (Need to be modified, TBD)

- **Error/Process Message.**

#	Short Name	Description	Possible FRUS
1	CMOS checksum error - Defaults loaded	Checksum of CMOS is incorrect, so the system loads the default equipment configuration. A checksum error may indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.	System board
2	CPU at nnnn	Displays the running speed of the CPU.	processor
3 4	Press ESC to skip memory test Floppy disk(s) fail	The user may press Esc to skip the full memory test. Cannot find or initialize the floppy drive controller or the drive. Make sure the controller is installed correctly. If no floppy drives are installed, be sure the Diskette Drive selection in Setup is set to NONE or AUTO.	System board system board
5	HARD DISK initializing Please wait a moment	Some hard drives require extra time to initialize.	System board
6	HARD DISK INSTALL FAILURE	Cannot find or initialize the hard drive controller or the drive. Make sure the controller is installed correctly. If no hard drives are installed, be sure the Hard Drive selection in Setup is set to NONE.	System board
7	Keyboard error or no keyboard present	Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are pressed during POST. To purposely configure the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. The BIOS then ignores the missing keyboard during POST.	System board
8	Memory Test:	This message displays during a full memory test, counting down the memory areas being tested.	DIMM System board

- **Check Point List**

POST (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
A1h	Set Initial Conditions (Default Values) in EBP
A2h	Determine FSB frequency.
A3h	Begin Detection of installed DIMMS
A4h	Check for Column Latency
A5h	200Mhz or 266Mhz
A6h	Check for tRAS timing
A7h	Check for tRP timing
A8h	Check for tRCD timing
A9h	Check for ECC Support
AAh	Check for refresh timing
ABh	Verify that the DIMM's are in matched pairs
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
01h	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved

10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.

2Ah	Reserved
2Bh 2Ch	Reserved Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, CPU speed …..
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh 40h	Reserved Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h 45h	Reserved Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program write allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch 4Dh	Reserved Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved

50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to “AUTO”.
6Eh	Reserved
6Fh	1.Initialize floppy controller 2.Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..

76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: wClear EPA or customization logo.
80h	Reserved
81h	Reserved
82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h 85h	Initialize ISA PnP boot devices 1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode 4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h FFh	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table. Boot attempt (INT 19h)

Check Point & Beep Code List

Bootblock Initialization Code Checkpoints

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processor (BSP) initialization like microcode update, frequency and other CPU critical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is disabled. Perform keyboard controller BAT test. Save power-on CPUID value in scratch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3 D4	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled. Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Performs main BIOS checksum and updates recovery status accordingly.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows to checkpoint E0. See *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9 DA	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM. Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is waking from ACPI S3 state
E1-E8 EC-EE	OEM memory detection/configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to the next.

Bootblock Recovery Code Checkpoints

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9 EA	Set up floppy controller and data. Attempt to read from floppy. Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.
FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST Code Checkpoints

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache – Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor
C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.

2A	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that has optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See *DIM Code Checkpoints* section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disable NMI as selected

90	Initialization of system management interrupts by invoking all handlers. *Please note this checkpoint comes right after checkpoint 20h*
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

Beep Codes

Boot Block Beep Codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

POST BIOS Beep Codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

Troubleshooting POST BIOS Beep Codes

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. · If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. · If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

PCI Configuration

PCI Interrupt Request Routing

The IRQ, acronym of interrupt request line and pronounced I-R-Q, are hardware lines over which devices can send interrupt signals to the microprocessor. The PCI IRQ pins are typically connected to the PCI bus pins as follows:

DEVICE	MCP1 INT Pin	IDSEL	CLOCK	REQ# / GNT#
PCI Slot	PIRQA	AD17	PCICLK 0	REQ#0 / GNT#0
Mini PCI Slot	PIRQB	AD18	PCICLK 1	REQ#1 / GNT#1
LAN1	PIRQC	AD21	CLKLAN 1	REQ#2 / GNT#2
LAN2	PIRQD	AD22	CLKLAN 2	REQ#3 / GNT#3

Resource List

I/O Map

I/O Port	Description
0000-000F	DMA Controller 1
0020-0021	Interrupt Controller 1
0040-0043	System Timer
004E-004F	SIO Port
0060,0064	Keyboard Controller
0070-0073	RTC and CMOS
0080-0090	DMA Controller Page Registers
0092	Port 92h
00A0-00A1	Interrupt Controller 2
00B2-00B3	APM register
00C0-00DF	DMA Controller 2
00F0-00FF	Numeric Data Processor
0170-0177	Secondary IDE Controller
01F0-01F7	Primary IDE Controller
02E8-02EF	COM4
02F8-02FF	COM2
0376	Secondary IDE Controller
0378-037F 03E8-03EF	LPT1 COM3
03F6	Primary IDE Controller
03F8-03FF	COM1
0400-045F	ACPI I/O space
0500-050F	SMBus I/O Space
0CF8-0CFF	PCI configuration Port

PCI Devices

Devices	Bus	Dev	Fun	ADSel	Ints
Host and AGP control	0	0	0	Internal	
Error Reporting	0	0	1	Internal	
Host Bus Control	0	0	2	Internal	
Dram Control	0	0	3	Internal	
Power Management Control	0	0	4	Internal	
North-South Module Interface Control	0	0	7	Internal	
PCI to PCI Bridge	0	1	0	Internal	
SATA and EIDE controller	0	15	0	Internal	
USB 1.1 UHCI Controllers	0	16	0~2	Internal	
USB 2.0 EHCI Controller	0	16	4	Internal	
Bus and Power Management Control	0	17	0	Internal	
South-North Module Interface Control	0	17	7	Internal	
PCI to PCIE Bridge	0	19	0	Internal	
PCI to PCI Bridge	0	19	1	Internal	
VIA VGA Controller	1	0	0	Internal	
Realtek Ethernet Controller	2	5	0	AD21	INT C
Realtek Ethernet Controller	2	6	0	AD22	INT D
VIA HDA Controller	128	0	0	Internal	
PCI Slot	2	1	0	AD17	INT A
Mini PCI Socket	2	2	0	AD18	INT B

SMBus Resource Allocation

Device	Address	Description
ICS952906	1101 001X	Clock Generator
MS-7	0101 111X	ACPI Controller
W83786NG	0101 110X	H/W Monitor
DIMM Slot	1010 0000	SPD

ISA Interrupt Allocation

IRQ	Description
IRQ0	System Timer
IRQ1	Keyboard Controller
IRQ2	Cascade Interrupt
IRQ3	COM2
IRQ4	COM1
IRQ5	COM3
IRQ6	COM4
IRQ7	LPT1
IRQ8	RTC
IRQ9	ACPI Controller Interrupt
IRQ10	PCI Device
IRQ11	PCI Device
IRQ12	PS/2 Mouse
IRQ13	Numeric Data Processor
IRQ14	Primary IDE Controller
IRQ15	Secondary IDE Controller

ISA DMA Channel Allocation

DMA Channel	Description
Channel 0	Unassigned 8-bit channel
Channel 1	Unassigned 8-bit channel
Channel 2	Unassigned 8-bit channel
Channel 3	Unassigned 8-bit channel
Channel 4	Cascade channel
Channel 5	Unassigned 16-bit channel
Channel 6	Unassigned 16-bit channel
Channel 7	Unassigned 16-bit channel

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