



integration with integrity

2808030 User's Manual

Mini-ITX Motherboard

Version 1.0



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Introduction

Product Description

The 2808030 Mini ITX board incorporates the Mobile Intel® 910GML/915GME Express Chipset for Embedded Computing, consisting of the Intel® 910GML/915GME Graphic Memory Controller Hub (GMCH) and Intel® I/O Controller Hub 6-M (ICH6-M), is an optimized integrated graphics solution with a 400/533MHz front-side bus.

The integrated 32-bit 3D graphics engine, based on Intel® Graphics Media Accelerator 900 (Intel® GMA 900) architecture, operates at core speeds of up to 320 MHz. It features a low-power design, is validated with Intel® Pentium M/Celeron® M processors on 130nm or 90nm process. With one DIMM socket on board, the board supports up to 1GB of DDR2 system memory (400MHz for 910GML, 400/533MHz for 915GME chipset).

Intel® Graphics supports a unique intelligent memory management scheme called Dynamic Video Memory Technology (DVMT). DVMT handles diverse applications by providing the maximum availability of system memory for general computer usage, while supplying additional graphics memory when a 3D-intensive application requests it. The Intel GMA 900 graphics architecture also takes advantage of the high-performance Intel processor. Intel GMA 900 graphics supports Dual Independent Display technology.

The main features of the board are:

- Supports Celeron® M processors, 400MHz FSB (910GML chipset)
- Supports Socket 479, 533/400MHz FSB (915GME chipset)
- One DDRII SDRAM DIMM supports up to 1GB of DDR2 400MHz (910GML chipset), DDR2 400/533MHz (915GME chipset)
- Onboard 10/100 BaseT and Marvell PCI-Express Gigabit LAN
- Intel® 915 Express VGA for CRT, SDVO port supports LVDS and DVI / LVDS
- 2x SATA, 6x USB 2.0, 4x COM, Watchdog timer
- 1x PCI, 1x MiniPCIe, CF socket, DC-in for +12V input

Dimensions of the board are 170mm x 170mm.

Checklist

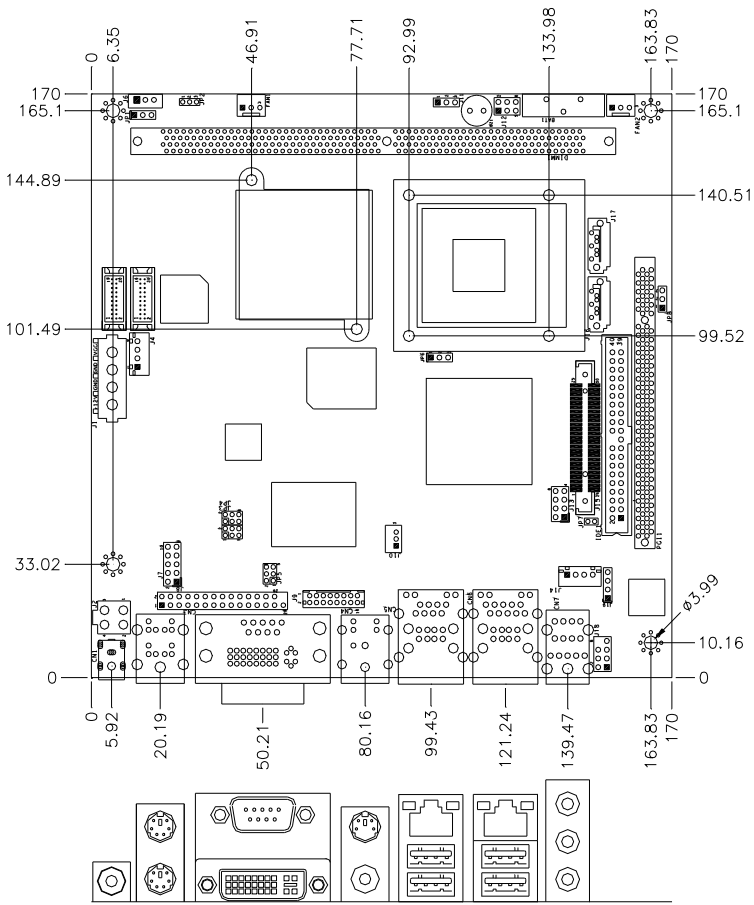
Your 2808030 package should include the items listed below.

- The 2808030 Celeron® M Mini-ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Cable kit (IDE, Serial port, Serial ATA, VGA)

2808030 Specifications

Form Factor	Mini ITX
CPU Type	Intel Celeron M / Pentium M (on Socket 479) processor (Banias or Dothan core): <ul style="list-style-type: none"> - Banias: ULV Celeron M 600MHz (512KB L2 Cache), - Dothan: Zero L2 cache Celeron M 1GHz or Celeron M 373
CPU Voltage	0.700V ~ 1.708V
CPU FSB	400MHz (910GML); 400/533MHz (915GME)
CPU Socket	Socket 479 co-layout with micro-FCBGA
Chipset	Intel 910GML/915GME chipset ICH6M: 82801FBM
BIOS /APM	Award BIOS, support ACPI Function & APM1.2
Memory	DDRII 400/533 SDRAM DIMM socket x1 (w/o ECC function), Max. 1GB
VGA	910GML built-in, supports dual display with CRT, LVDS & TV-Out
DVI	Chrontel CH7307 x1 for DVI
LVDS	Chrontel CH7308 x1 for 18 or 24-bit single/dual channel LVDS
LAN	LAN1: ICH6M built-in 10/100BT MAC + Intel 82562ET PHY Optional LAN2: Marvell 88E8053 PCI Express Gigabit LAN controller
USB	ICH6M built-in USB 2.0 host controller, support 6 ports
Serial ATA	ICH6M built-in SATA controller, supports 2 ports
Parallel IDE	ICH6M built-in one channel Ultra DMA 33/66/100 for IDE & CF
Audio	ICH6M built-in Audio controller + AC97 Codec ALC655 w/ 6 channels (Line-out, Line-in & Mic.) + ADI SSM2304 4ohm 2W, class D, stereo audio power amplifier (note: 1.4W for 8 ohm)
LPC I/O	Winbond W83627EHG: PS/2 Keyboard/Mouse, 2x serial (RS232) & Hardware monitor (3 thermal inputs, 4 voltage monitor inputs, VID0-4 & 2 fan headers)
2 nd I/O	Fintek F81216DG x1 for COM3, 4 (RS-232)
Expansion Slots	PCI (33MHz/32-bit) slot x1 Optional Mini PCI-express (1 lane) socket x1 (for wireless module)
Edge Connectors	DC-in power connector (Jack type) x1 PS/2 stack connector x1 for keyboard/mouse DVI + DB9 stack connector x1 for DVI & COM 1 RJ45 (10/100) + dual USB stack connector x1 for LAN1 & USB1, 2 S-Video connector x1 for S-Video RJ45 (GbE) + dual USB stack connector x1 for LAN2 & USB3, 4 *** Option with dual USB stack connector (LAN2 option) 3x1 phone jack stack connector x1 for Audio (Line-Out, Line-In & Mic)
Onboard Headers / Connectors	Compact flash socket (vertical type) x1 @component side SATA connector x2 for 2 SATA ports DF13-20 (20-pin) header x2 for LVDS 15 pins pin-header x1 for VGA 40 pins box-header x1 for IDE 30 pins pin-header x1 for COM2~4 8 pins pin-header x1 for USB 5-6 3 pins pin-header x1 for power LED 6 pins pin-header x1 for Reset, HDD LED & power button
Watchdog Timer	Yes (256 segments, 0, 1, 2...255 sec/min)
System Voltage	+5V, +3.3V, +12V, -12V, 5VSB
Other	LAN Wakeup
Digital I/O	4 in + 4 out (TTL level)
Power In / Out	Power Input: +12V DC power input Power Output: 4-pin power connector x1 for HDD/CD-ROM/DVD
Board Size	170mm x 170mm

Board Dimensions



Installations

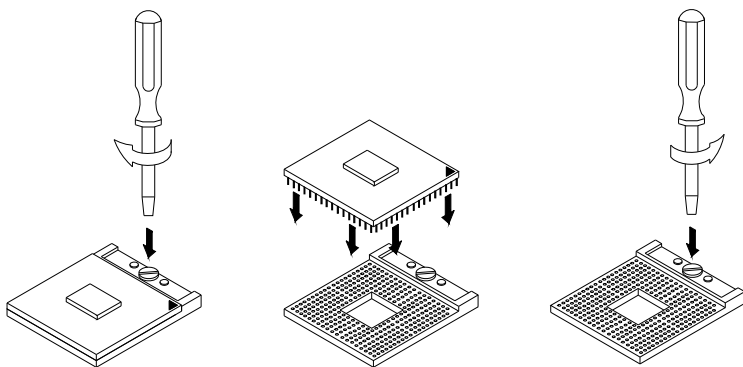
This section provides information on how to use the jumpers and connectors on the 2808030 in order to set up a workable system. The topics covered are:

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Installing the CPU

The 2808030 board supports a Socket 479 processor socket for Intel® Pentium® M or Celeron® M processors.

The processor socket comes with a screw to secure the processor. As shown in the left picture below, loosen the screw first before inserting the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, fasten the screw. Refer to the figures below.



NOTE: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.

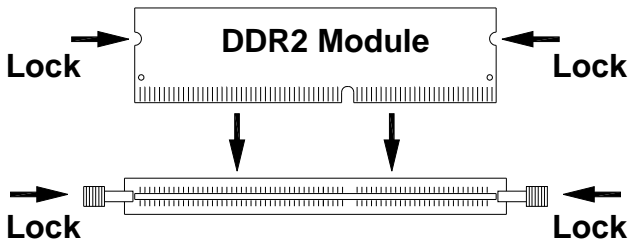
Installing the Memory

The 2808030 board supports one DDR2 memory socket for a maximum total memory of 1GB in DDR2 memory type.

Installing and Removing Memory Modules

To install the DDR2 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR2 module so that the key of the DDR2 module align with those on the memory slot.
2. Gently push the DDR2 module in an upright position until the clips of the slot close to hold the DDR2 module in place when the DDR2 module touches the bottom of the slot.
3. To remove the DDR2 module, press the clips with both hands.

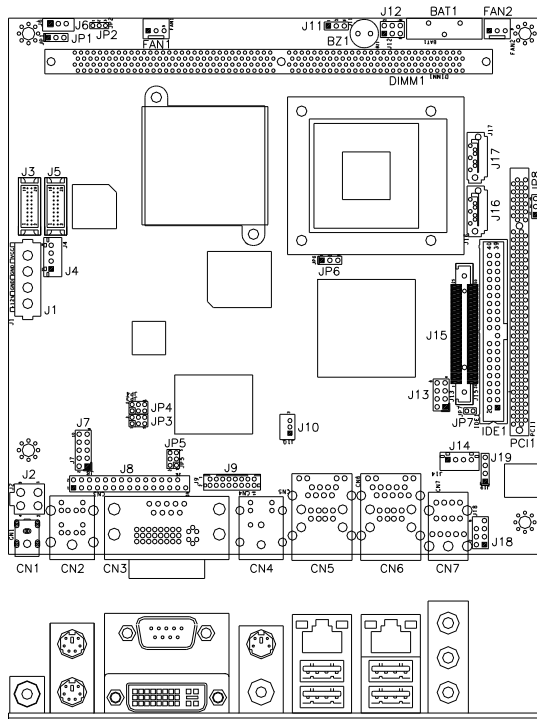


Setting the Jumpers

Jumpers are used on 2808030 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on 2808030 and their respective functions.



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JP7: CompactFlash Slave/Master Selection.....	10
JP2: ATX/AT Mode Select.....	10
JP3: COM3 RS232 +5V / +12V Power Setting.....	10
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Jumper Locations on 2808030





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

JP1: LCD Panel Power Selection

JP1	LCD Panel Power
	3.3V
	5V



JP8: Clear CMOS Setting

JP8	Setting
	Normal
	Clear CMOS


JP7: CompactFlash Slave/Master Selection

JP7	CF Setting
 Short	Master
 Open	Slave

JP2: ATX/AT Mode Select

JP2	ATX / AT
	ATX mode
	AT mode

JP3: COM3 RS232 +5V / +12V Power Setting

Pin #	Signal Name	JP3	Signal Name	Pin #
1	RI		+12V	2
3	RI (Default)		RI (Default)	4
5	RI		+5V	6

COM3 Settings: Pin 1-2 short = +12V, Pin 5-6 short = +5V, Pin 3-4 Standard COM Port

JP4: COM4 RS232 +5V / +12V Power Setting

Pin #	Signal Name	JP4	Signal Name	Pin #
1	RI		+12V	2
3	RI (Default)		RI (Default)	4
5	RI		+5V	6

COM4 Settings: Pin 1-2 short = +12V, Pin 5-6 short = +5V, Pin 3-4 Standard COM Port

JP5: VGA/DVI DDCDATA and DDCCLK Signal Select

JP5	VGA/DVI Select
	VGA
	DVI

JP6: CPU FSB Selection (915GME only)

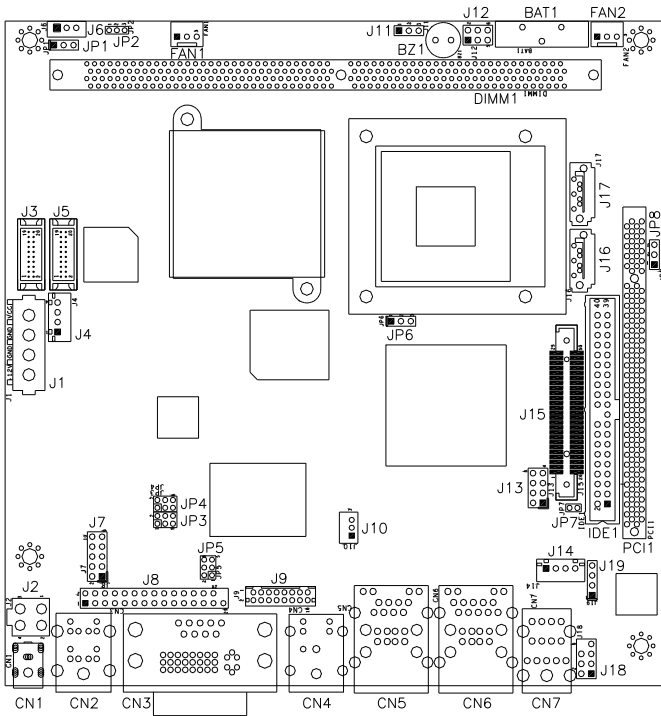
JP6	FSB
	400MHz
	533MHz

Connectors on 2808030

The connectors on 2808030 allows you to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc. The following table lists the connectors on 2808030 and their respective functions.

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J19: CD-In Pin Header	20
PCI1: PCI Slot (supports 2 Master).....	20
U38: Mini PCI- E(x1) Connector (bottom side).....	20

Connector Locations on 2808030



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J19: CD-In Pin Header.....	20
PC11: PCI Slot (supports 2 Master)	20
U38: Mini PCI-E(x1) Connector (bottom side).....	20

FAN1: CPU Fan Power Connector

FAN1 is a 3-pin header for the CPU fan. The fan must be a 12V fan.



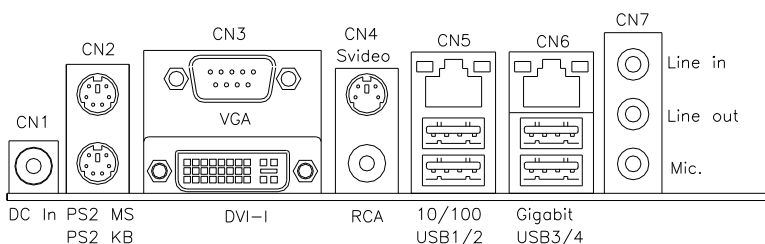
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

FAN2: System Fan Power Connector

FAN2 is a 3-pin header for system fans. The fan must be 12V (500mA).

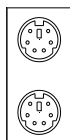


Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection



CN1: DC Jack (DC in, 12V only)

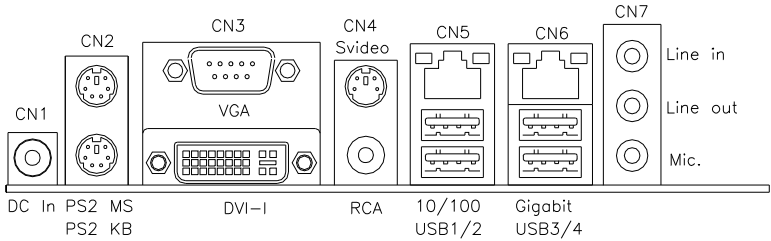
CN2: PS/2 Keyboard and PS/2 Mouse Connectors



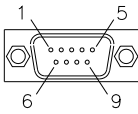
PS/2 Mouse

PS/2 Keyboard

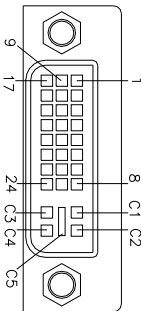
Signal Name	Keyboard	Mouse	Signal Name
Keyboard data	1	1	Mouse data
N.C.	2	2	N.C.
GND	3	3	GND
5V	4	4	5V
Keyboard clock	5	5	Mouse clock
N.C.	6	6	N.C.



CN3: COM1 and DVI-I Connector



Signal Name	Pin #	Pin #	Signal Name
DCD	1	6	DSR
RXD	2	7	RTS
TXD	3	8	CTS
DTR	4	9	RI
GND	5	10	Not Used



Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
VSYNC	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	A RED
SHIELD 1/3	11	C2	A GREEN
DATA 3-	12	C3	A BLUE
DATA 3+	13	C4	HYNC
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3

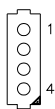
CN4: S-Video and RCA Connector for TV out

CN5: 10/100 RJ-45 and USB1/2 Ports

CN6: GbE RJ-45 and USB3/4 Ports

CN7: Audio Connector

J1: HDD Power Connector



Pin #	Signal Name
1	+12V
2	Ground
3	Ground
4	5V

Note: +12V power is provided with 2A maximum load.

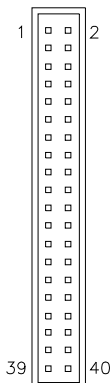
J2: ATX_12V Connector

J2 can be used in situations where the 12V current from the ATX power is insufficient to supply needed current.



Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

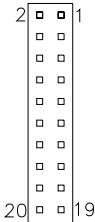
IDE1: IDE Connector



Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Protect pin
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground


J3, J5: LVDS Connectors (1st channel, 2nd channel)

The LVDS connectors on board consist of the first channel (J3) and second channel (J5) and supports 18-bit or 24-bit.



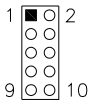
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

J6: LCD Backlight Connector



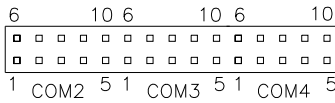
Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Ground

J7: Digital I/O



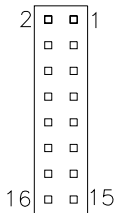
Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J8: COM2, COM3, COM4 Serial Ports



Pin #	Signal Name (RS-232)
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	Ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator
10	No Connect.

J9: VGA Connector



Signal Name	Pin #	Pin #	Signal Name
+5V	2	1	RED
Ground	4	3	GREEN
N.C.	6	5	BLUE
SDA	8	7	N.C.
HSYNC	10	9	Ground
VSYNC	12	11	Ground
SCL	14	13	Ground
N.C.	16	15	Ground

J10: Wake On LAN Connector

J10 is a 3-pin header for the Wake On LAN function. Wake On LAN will function properly only with an ATX power supply with 5VSB that has 200mA.



Pin #	Signal Name
1	+5VSB
2	Ground
3	-PME

J11: Power LED Connector

Pin #	Signal Name
1	Vcc
2	NC
3	PLED

J12: System Function Connector

Signal Name	Pin	Pin	Signal Name
Ground	1	2	PS_ON
5V	3	4	HDD Active
Ground	5	7	Reset

ATX power on switch: Pins 1-2

HDD LED: Pins 3-4

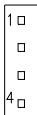
Reset switch: Pins 5-6

J13: USB5/6 Port Pin Header

Signal Name	Pin	Pin	Signal Name
Vcc	1	5	Ground
D-	2	6	D+
D+	3	7	D-
Ground	4	8	Vcc

J14: Speaker Connector

The J14 connector supports 2W/8ohm stereo audio power amplifier.



Pin #	Signal Name
1	Audio L
2	Ground
3	Ground
4	Audio R

J15: Compact Flash Connector**J16, J17: Serial ATA Connectors**

J18: Front Audio Connector



Signal Name	Pin	Pin	Signal Name
Rear Audio R	1	5	Rear Audio L
Front Audio R	2	6	Front Audio L
Mic In	3	7	VREF Out
Ground	4	8	

REMARKS: To use the front audio connector, the jumpers on pin 1-3 and pin 2-4 must be removed.

J19: CD-In Pin Header



Pin #	Signal Name
1	CD Audio R
2	Ground
3	Ground
4	CD Audio L

PCI1: PCI Slot (supports 2 Master)

U38: Mini PCI- E(x1) Connector (bottom side)

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=====
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
#include <stdio.h>
#include <stdlib.h>
#include "W627EHF.H"
//=====
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=====
int main (int argc, char *argv[])
{
    unsigned char bBuf;
    unsigned char bTime;
    char **endptr;

    copyright();

    if (argc != 2)
    {
        printf(" Parameter incorrect!!\n");
        return 1;
    }

    if (Init_W627EHF() == 0)
    {
        printf(" Winbond 83627HF is not detected, program abort.\n");
        return 1;
    }
    bTime = strtol (argv[1], endptr, 10);
    printf("System will reset after %d seconds\n", bTime);

    EnableWDT(bTime);

    return 0;
}
//=====
```

```
void copyright(void)
{
    printf("\n===== Winbond 83627EHF Watch Timer Tester (AUTO DETECT) =====\n")
        " Usage : W627E_WD reset_time\n"
        " Ex : W627E_WD 3 => reset system after 3 second\n"
        "       W627E_WD 0 => disable watch dog timer\n");
}
//=====
void EnableWDT(int interval)
{
    unsigned char bBuf;

    bBuf = Get_W627EHF_Reg( 0x2D);
    bBuf &= (10x01);
    Set_W627EHF_Reg( 0x2D, bBuf);           //Enable WDTO

    Set_W627EHF_LD( 0x08);                 //switch to logic device 8
    Set_W627EHF_Reg( 0x30, 0x01);         //enable timer

    bBuf = Get_W627EHF_Reg( 0xF5);
    bBuf &= (10x08);
    Set_W627EHF_Reg( 0xF5, bBuf);         //count mode is second

    Set_W627EHF_Reg( 0xF6, interval);     //set timer
}
//=====
void DisableWDT(void)
{
    Set_W627EHF_LD(0x08);                 //switch to logic device 8
    Set_W627EHF_Reg(0xF6, 0x00);         //clear watchdog timer
    Set_W627EHF_Reg(0x30, 0x00);         //watchdog disabled
}
//=====
```

```
//=====
//
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// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
#include "W627EHF.H"
#include <dos.h>
//=====
unsigned int W627EHF_BASE;
void Unlock_W627EHF (void);
void Lock_W627EHF (void);
//=====
unsigned int Init_W627EHF(void)
{
    unsigned int result;
    unsigned char ucDid;

    W627EHF_BASE = 0x2E;
    result = W627EHF_BASE;

    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {
        goto Init_Finish;
    }

    W627EHF_BASE = 0x4E;
    result = W627EHF_BASE;
    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {
        goto Init_Finish;
    }

    W627EHF_BASE = 0x00;
    result = W627EHF_BASE;
}

Init_Finish:
    return (result);
}
//=====
void Unlock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
}
//=====
void Lock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_LOCK);
}
//=====
void Set_W627EHF_LD( unsigned char LD)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, W627EHF_REG_LD);
    outportb(W627EHF_DATA_PORT, LD);
    Lock_W627EHF();
}
}
```

```

=====
void Set_W627EHF_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    outportb(W627EHF_DATA_PORT, DATA);
    Lock_W627EHF();
}
=====
unsigned char Get_W627EHF_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    Result = inportb(W627EHF_DATA_PORT);
    Lock_W627EHF();
    return Result;
}
=====

=====
//
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// PURPOSE.
//
=====
#ifndef __W627EHF_H
#define __W627EHF_H                1
=====
#define    W627EHF_INDEX_PORT      (W627EHF_BASE)
#define    W627EHF_DATA_PORT      (W627EHF_BASE+1)
=====
#define    W627EHF_REG_LD          0x07
=====
#define W627EHF_UNLOCK              0x87
#define    W627EHF_LOCK            0xAA
=====
unsigned int Init_W627EHF(void);
void Set_W627EHF_LD( unsigned char);
void Set_W627EHF_Reg( unsigned char, unsigned char);
unsigned char Get_W627EHF_Reg( unsigned char);
=====
#endif //__W627EHF_H

```

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support your products, projects and business.



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