



integration with integrity

2808050 User's Manual

Industrial Motherboard with Socket LGA 775

Version 1.0

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Ordering Information:

Model	ICH	SATA	Intel LANPHY	PCI-E Gigabit LAN	Remarks
Remarks					
2808050A	ICH9	4	82562V/ 10/100	N/A	
2808050B	ICH9	4	82566DM(1G)	PCI-E GbE	
2808050C	ICH9	4	82566DM(1G)	PCI-E GbE	PCB thickness: 2.5mm;
2808050D	ICH9R (RAID)	6	82566DM/(1G)	PCI-E GbE	

Introduction

Checklist

Your 2808050 motherboard package should include the items listed below:

- The 2808050 motherboard
- This User's manual
- 1 Back I/O shield
- 1 IDE cable
- 1 Floppy cable
- 1 SATA cable
- 1 Serial-Port cable
- 1 CD containing the following:
 - Chipset Drivers
 - Flash Memory Utility

Reminder:

About IDE

The IDE connector on board does not support OS installation in hard drive. A system hard drive connected to this IDE cannot be booted up to OS.

About SATA

When using a legacy operating system, only one SATA controller is available that supports SATA port 0 – 3 (CN8, CN9, CN10, CN11). It is suggested that the legacy operating system is installed using any of these ports.

Product Description

The 2808050 LGA 775 motherboard incorporates the Intel Q35 chipset that can utilize a single LGA775 processor of up to 4.0GHz or higher and supports FSB frequency of 800/1066MHz/1333MHz (200MHz(800MT/s) and 266MHz(1066MT/s), 333MHz(1333MT/s) HCLK respectively.

The Q35 chipset is designed for use with the Core.2 processor family, including a faster 1333 MHz system bus. The integrated GMCH component provides the CPU interface, DDR2 interface, Hub Interface and PCI Express graphics interface.

Four DDR2 memory sockets support DDR2 667/800 SDRAM DIMM modules of up to 8GB in capacity.

The board is designed with one Intel 82566DM PCI Express Gigabit PHY or 82562V 10/100 PHY LAN controllers. Serial-II ATA connectors offer 3Gb/s data throughput speed - faster than the most advanced parallel ATA.

Expansion includes four PCI slots, one PCI Express x1 and one PCI Express x16 and one ISA slot. Other advanced features include ten USB 2.0 ports, IrDA interface, digital I/O, four serial ports, watchdog timer and audio function. Dimensions of the board are 12" by 9.5" in an ATX form factor.

Remarks: 2808050 supports Intel Supports the Intel Core 2 Duo and Intel Core 2 Quad processors, and Intel Celeron 400(Conroe-L) Sequence processor.

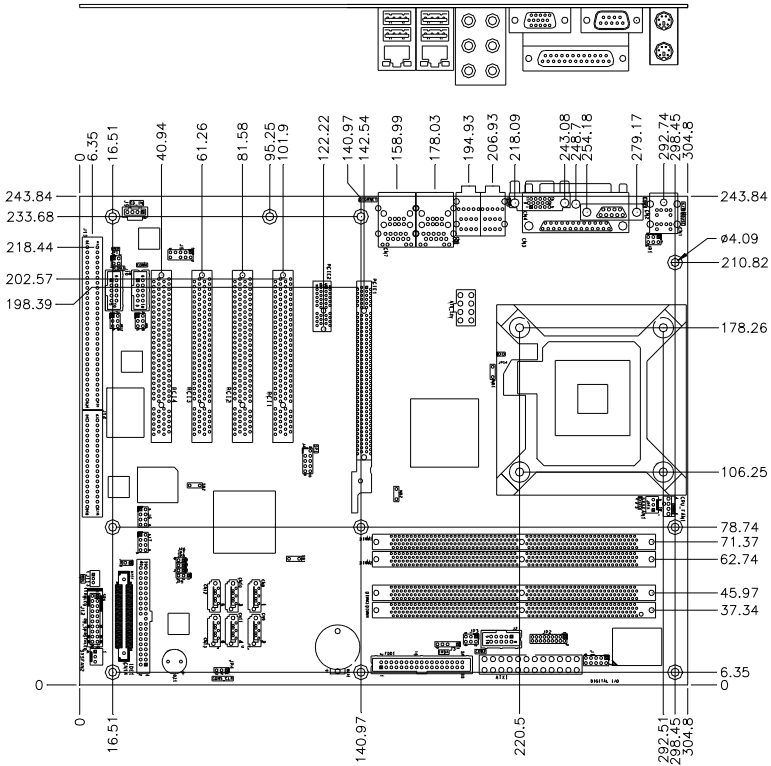
2808050D supports six Serial ATA connectors (with RAID function). 2808050 A, B, C supports four Serial ATA connectors only. 2808050C has the same specifications as 2808050B, except that its PCB thickness is 2.4mm).

The IDE connector on board does not support OS installation in hard drive. A system hard drive connected to this IDE cannot be booted up to OS.

Specifications

Product Name	2808050
CPU Support	Socket LGA775, Supports the Intel Core 2 Duo and Intel Core2 Quad processors, and Intel Celeron 400 (Conroe-L) Sequence processor.
CPU Voltage	0.5V~1.6V (VRD 11.0)
System Speed	Up to 3.8GHz+
CPU FSB	800MHz/1066MHz /1333MHz
Green /APM	APM1.2
CPU Socket	LGA 775
Chipset	Intel® Bearlake Chipset Q35+ICH9 for 2808050 A, B, C Q35+ICH9R for 2808050D only
BIOS	Award BIOS; supports ACPI
VGA	Q35 built-in, supports CRT
LAN1	LAN1: Dual footprint support option *Intel 82566DM PCI Express Gigabit for 2808050 B, C, *Intel 82562V PHY 10/100 for 2808050A only Marvell PCI Express Gigabit for 2808050 B, C, D
LAN2	ICH9/ICH9R Built-in audio + HDA codec
Audio	
Memory type	Support Dual Channel DDR2 DIMM Module x 4, 667/800MHz (Without ECC function), Max. 8GB
LPC I/O	W83627EHG: IrDA x1, Parallel x1, COM1 (RS232), COM2 (RS232/422/485), FDCx1, Hardware monitoring
RTC/CMOS	Built in ICH9/ICH9R
Battery	Lithium battery
Keyboard Controller	Built-in Winbond 83627EHG
PATA	JMicro JMB368 PCI-E to PATA controller for one PATA channel support One PATA : IDE connectorx1 +Compact Flash socket Type II x1 IDE1(40pin/2.5mm)supports Ultra DMA 33/66/100 compact Flash (use IDE or CF at a time only)
SATA2 connector	2808050 A, B, C supports 4x SATA2 (300MB/s) 2808050D supports 6x SATA2 with RAID function
D-type connectors	PS/2 mouse, PS/2 KB, VGA (CRT), RJ-45, Sound, USB x 4
Power Connector	ATX 24-pin
Expansion Slots	1 x (PCI Express x16) slot, 1 x (PCI Express x1) slot 4 x PCI slots, 1 x ISA slots (slave only), cannot support ISA master and DMA access function
PCI to ISA Bridge	Winbond W83628F with W83629D
Secondary Super I/O	Fintek F81216, supports COM3, COM4 (RS232)
USB	ICH9 built in USB Version 2.0, support 8 ports (D-type connector x 4 port & pin header x 4 port)
Digital I/O	4 In, 4 Out
Watchdog Timer	Supports 256 segments (0,1,2...255. Sec/min)
System Voltages	+5V, +12V, -12V, 5VSB, -5V, 3.3V
Board Size	12" x 9.5" (ATX form factor)
Other Features	IrDA interface, Modem Wakeup,
Dimensions	305mm x 244mm (12" x 9.6")

Board Dimensions



Installations

This section provides information on how to use the jumpers and connectors on the 2808050 in order to set up a workable system. The topics covered are:

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Installing the Memory	8
Setting the Jumpers	9
Connectors on 2808050.....	14
Watchdog Timer Configuration	28

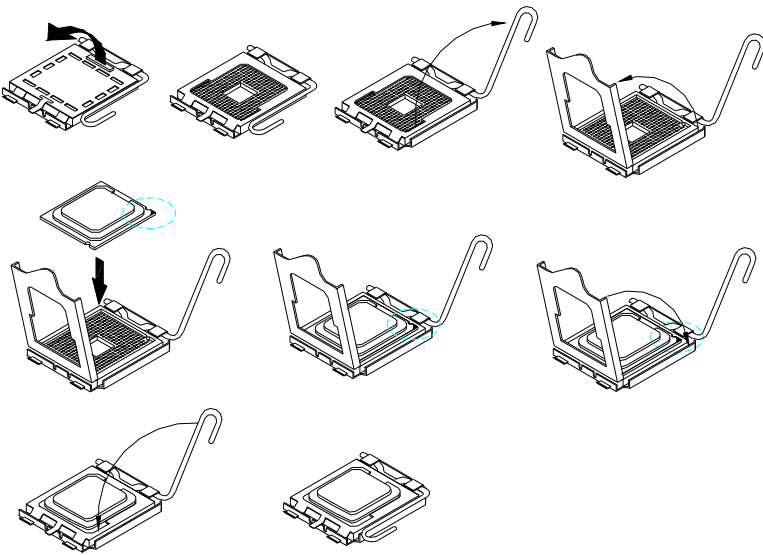
Reminder:

The IDE connector on board does not support OS installation in hard drive. A system hard drive connected to this IDE cannot be booted up to OS.

Installing the CPU

The 2808050 motherboard support an LGA 775 processor socket for Intel Core 2 Duo and Intel Core2 Quad processors, and Intel Celeron 400(Conroe-L) Sequence processor.

The LGA 775 processor socket comes with a lever to secure the processor. Refer to the pictures below, from left to right, on how to place the processor into the CPU socket. ***Please note that the cover of the LGA775 socket must always be installed during transport to avoid damage to the socket.***



ATX Power Installation

The system power is provided to the motherboard with the ATX1 and ATX_12V power connectors. ATX1 is a 24-pin power connector and ATX_12V is a 8-pin 12V power connector.

The 24-pin power connector can to be connected to a standard 20-pin ATX power connector in a standard ATX power supply (Min. 400watt).

Note: The power supply 5VSB voltage must be at least 2A.

Installing the Memory

The 2808050 motherboard support four DDR2 memory sockets for a maximum total memory of 8GB in DDR memory type. It supports DDR2 667/800.

Basically, the system memory interface has the following features:

- Supports two 64-bit wide DDR data channels
- Available bandwidth up to 6.4GB/s (DDR2 800) for single-channel mode and 12.8GB/s (DDR2 800) in dual-channel mode.
- Supports 256Mb, 512Mb, 1Gb DDR2 technologies.
- Supports only x8, x16, DDR2 devices with four banks
- Supports only unbuffered DIMMs
- Supports opportunistic refresh
- Up to 32 simultaneously open pages (four per row, four rows maximum)

Dual Channel Memory Configuration

If you want to operate the Dual Channel Technology, please note the following explanations due to the limitation of Intel chipset specifications.

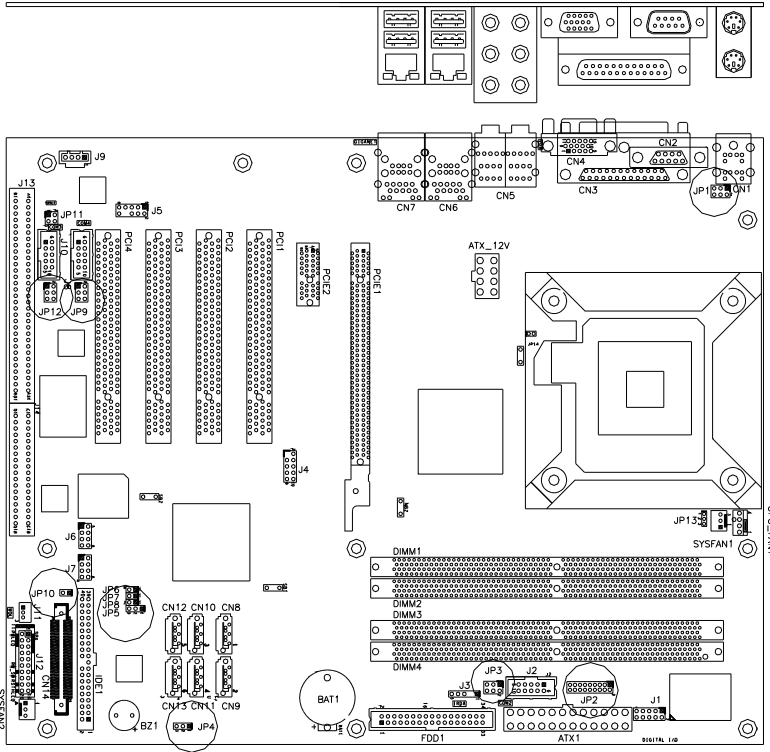
1. Dual Channel mode will not be enabled if only one DDR II memory module is installed.
2. To enable Dual Channel mode with two or four memory modules (it is recommended to use memory modules of identical brand, size, chips, and speed), you must install them into DIMM sockets of the same color. The following is a Dual Channel Memory configuration table: (DS: Double Side, SS: Single Side)

	DDR11	DDR12	DDR13	DDR14
2MemoryModules	DS/SS	X	DS/SS	X
	X	DS/SS	X	DS/SS
4MemoryModules	DS/SS	DS/SS	DS/SS	DS/SS

Setting the Jumpers

Jumpers are used on 2808050 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on 2808050 and their respective functions.

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JP4: Clear CMOS Contents	12
JP5: Configure and Recovery (Factory use only).....	12
JP8: ME (Management Engine) – Disabled / pin closed.....	12
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JP12: COM3 RS232 +5V/+12V Power Setting	13



Jumper Locations Page

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JP2: RS232/422/485 (COM2) Selection..... 11

JP3: COM2 RS232 +5V/+12V Power Setting..... 11

JP4: Clear CMOS Contents 12

JP5: Configure and Recovery (Factory use only)..... 12

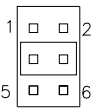
JP8: ME (Management Engine) – Disabled / pin closed 12

JP9: COM4 RS232 +5V/+12V Power Setting..... 12

JP10: Compact Flash Socket Master/Slave Setting 13

JP12: COM3 RS232 +5V/+12V Power Setting..... 13

JP1: COM1 RS232 +5V/+12V Power Setting


JP1	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	Normal
	Pin 5-6 Short/Closed	+5V

JP2: RS232/422/485 (COM2) Selection

COM1 is fixed for RS-232 use only.

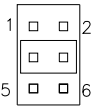
JP2, COM2 is selectable for RS232, RS-422 and RS-485.

The following table describes the jumper settings for COM2 selection.

COM2 Function	RS-232	RS-422	RS-485	
	Short: 1-2	Short: 3-4	Short: 5-6	
	Jumper Setting (pin closed)	9-11	7-9	7-9
		10-12	8-10	8-10
		15-17	13-15	13-15
		16-18	14-16	14-16



Note: Factory is default RS-232

JP3: COM2 RS232 +5V/+12V Power Setting




JP3	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	Normal
	Pin 5-6 Short/Closed	+5V

JP4: Clear CMOS Contents

Use JP4, a 3-pin header, to clear the CMOS contents. *Note that the ATX-power connector should be disconnected from the motherboard before clearing CMOS.*

JP4	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

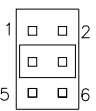
JP5: Configure and Recovery (Factory use only)

JP5	Setting	Function
	Pin 1-2 Short/Closed	Normal (default)
	Pin 2-3 Short/Closed	Configure
	Open	Recovery



JP8: ME (Management Engine) – Disabled / pin closed

The factory default setting of the 2-pin JP8 jumper is closed. This means the management engine function is disabled.

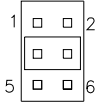
JP9: COM4 RS232 +5V/+12V Power Setting

JP9	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	Normal
	Pin 5-6 Short/Closed	+5V

JP10: Compact Flash Socket Master/Slave Setting

JP10	Compact Flash
 Short	Master
 Open	Slave

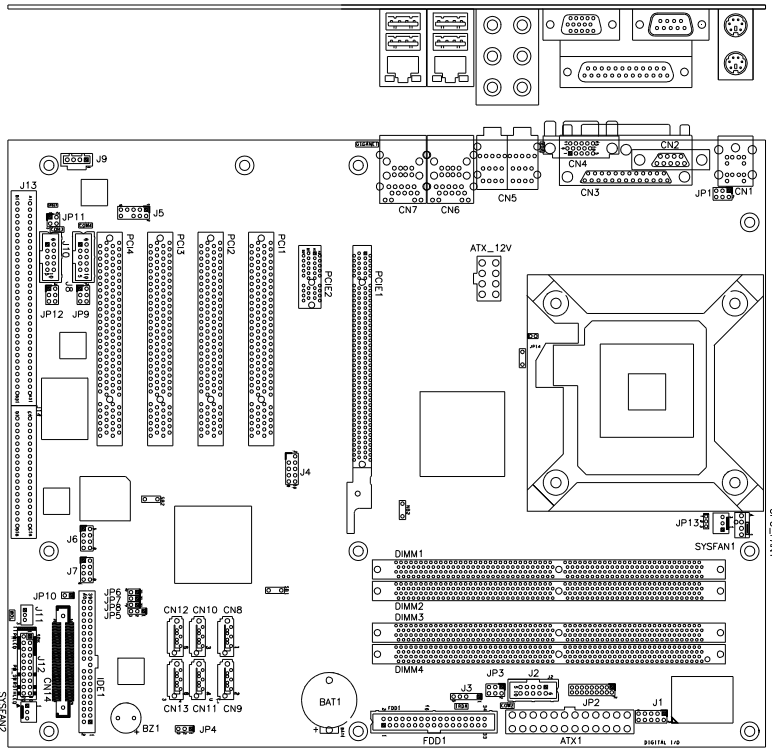
JP12: COM3 RS232 +5V/+12V Power Setting

JP12	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	Normal
	Pin 5-6 Short/Closed	+5V

Connectors on 2808050

The connectors on 2808050 allow you to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc.

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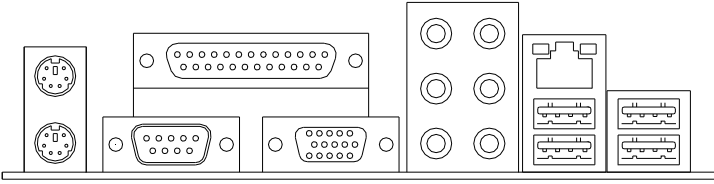


Connectors on 288050 A, B, C, D

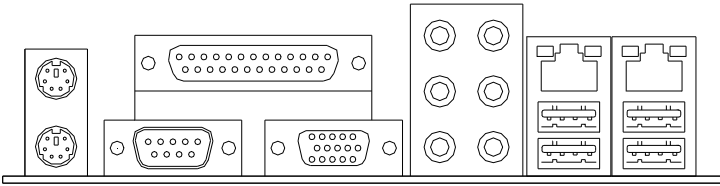
ATX1: 24-pin ATX Power Connector
 ATX_12V1: ATX 12V Power Connector
 DIMM1,2: Channel A DDR2 Socket
 DIMM3,4 Channel B DDR2 Socket
 CN1: PS/2 Keyboard and PS/2 Mouse
 CN2: Serial Ports(COM1)
 CN3: Parallel Port Connector
 CN4: VGA CRT Connector
 CN5: HD Audio Connector
 CN6: 10/100 RJ-45&USB 0/1 (288050A)
 CN6: GbE RJ-45 &USB 0/1
 (288050 B, C, D)
 CN7: USB2/3 Connector (288050A)
 CN7: GbE RJ-45&USB2/3
 (288050 B, C, D)
 CN8, CN9, CN10, CN11, CN12,CN13 SATA
 CN14: Compact Flash TYPE II Socket
 J1: Digital I/O Connector (4 in, 4 out)
 J2: COM2 Serial Port
 LED1: DRAM POWER LED Indicator

J3: IrDA Connector
 J4: SPI Debug Tools Port (Factory use only)
 J5: Audio Front Header
 J6: USB6/USB7 Connector
 J7: USB4/USB5 Connector
 J8, J10: COM3, COM4 Serial Ports(RS232)
 J9: CD-In Audio Connector
 J11: Wake On LAN Connector
 J12: System Function Connector
 J13: ISA Slot
 JP11: SPDIFI/ SPDIFO Connector (Reserved)
 IDE1: Primary IDE Connectors
 CPU_FAN1: CPU Fan Power Connector
 SYS_FAN1: system Fan1 Power Connector
 SYS_FAN2: SYSTEM Fan2 Power Connector
 FDD1: Floppy Drive Connector
 PCIE_1: x16 PCI Express Slot
 PCIE_2: x1 PCI Express Slots
 PC11, PC12, PC13, PC14: PCI Slots

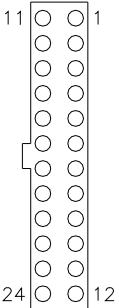
2808050A Edge Connectors



2808050 B, C, D Edge Connectors

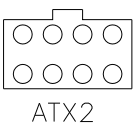


ATX1: 24-pin ATX Power Connector



Signal Name	Pin #	Pin #	Signal Name
3.3V	13	1	3.3V
-12V	14	2	3.3V
Ground	15	3	Ground
PS-ON	16	4	+5V
Ground	17	5	Ground
Ground	18	6	+5V
Ground	19	7	Ground
-5V	20	8	Power good
+5V	21	9	5VSB
+5V	22	10	+12V
+5V	23	11	+12V
Ground	24	12	+3.3V

ATX_12V1: ATX 12V Power Connector



Signal Name	Pin #	Pin #	Signal Name
+12V	5	1	Ground
+12V	6	2	Ground
+12V	7	3	Ground
+12V	8	4	Ground

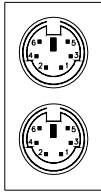
DIMM1, 2: Channel A DDR2 Socket

DIMM1, 2 are the first-channel DDR2 sockets.

DIMM3, 4 Channel B DDR2 Socket

DIMM3, 4 are the second-channel DDR2 sockets.

CN1: PS/2 Keyboard and PS/2 Mouse Connectors

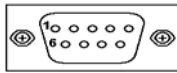


Mouse (top)
Keyboard (bottom)

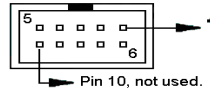
Keyboard Signal	Pin #	Mouse Signal
Keyboard data	1	Mouse data
N.C.	2	N.C.
GND	3	GND
5V	4	5V
Keyboard clock	5	Mouse clock
N.C.	6	N.C.

CN2: Serial Ports(COM1)

CN2 (COM1) is a DB-9 connector, while J2, J8 and J10 are COM pin-header connectors.



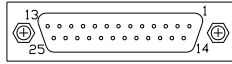
COM1 (DB-9)



Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

CN3: Parallel Port Connector

CN3 is a DB-25 external connector situated on top of the VGA and serial ports.

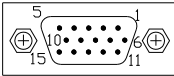


CN3 Parallel Port

Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	AutoFeed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	N/A	N/A

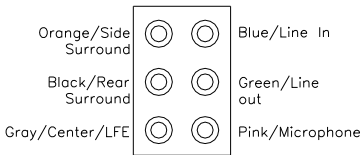
CN4: VGA CRT Connector

CN4 is a DB-15 VGA connector located beside the COM1 port. The following table shows the pin-out assignments of this connector.

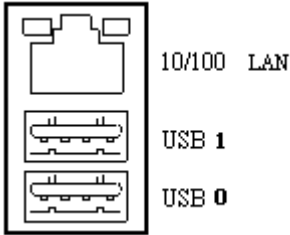


Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
VCC	9	10	GND
N.C.	11	12	DDCDATA
HSYNC	13	14	VSYNC
DDCCLK	15		

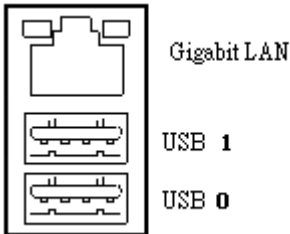
CN5: HD Audio Connector



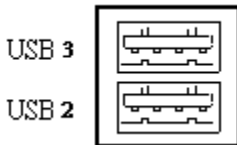
CN6: 10/100 RJ-45&USB 0/1 Connector (2808050A)



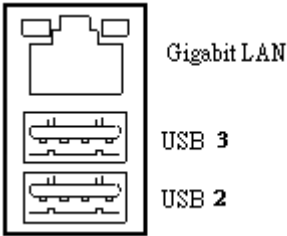
CN6: GbE RJ-45 &USB 0/1 Connector (2808050 B, C, D)



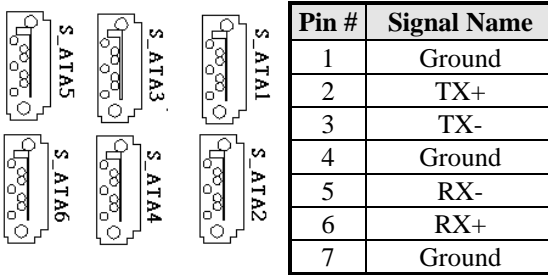
CN7: USB2/3 Connector (2808050A)



CN7: Marvell GbE RJ-45&USB2/3 Connector (2808050 B, C, D)



CN8, CN9, CN10, CN11, CN12, CN13 SATA Connector



*Note: 2808050 A, B, C supports 4x SATA II (300MB/s), S_ATA1,2,5,6 .
2808050D supports 6x SATA II with RAID function, S_ATA1,2,3,4,5,6.*

CN14: Compact Flash Type II Socket

Note: The CompactFlash interface cannot be used simultaneously with the IDE interface.

J1: Digital I/O Connector (4 in, 4 out)

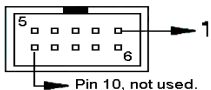
This 10-pin digital I/O connector supports TTL levels and is used to control external devices requiring ON/OFF circuitry.

The diagram shows a 10-pin connector with pins numbered 1 to 10. Pin 1 is a square, while pins 2 through 10 are circles.

Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	+5V
Out3	3	4	Out1
Out2	5	6	Out0
IN3	7	8	IN1
IN2	9	10	IN0

J2: COM2 Serial Port

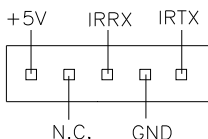
COM2 is jumper selectable for RS-232, RS-422 and RS-485.



Please refer to JP2: RS232/422/485 (COM2) Selection

Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	RTS-	NC
7	RTS	RTS+	NC
8	CTS	CTS+	NC
9	RI	CTS-	NC
10	NC	NC	NC

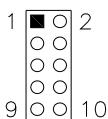
J3: IrDA Connector



Pin #	Signal Name
1	+5V
2	No connect
3	Ir RX
4	Ground
5	Ir TX

J4: SPI Debug Tools Port (Factory use only)

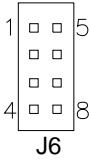
J5: Audio Front Header



Signal Name	Pin #	Pin #	Signal Name
MIC2_L	1	2	Ground
MIC2_R	3	4	Presence#
Line2_R	5	6	MIC2_ID
Sense	7	8	NC
Line2_L	9	10	Line2_ID

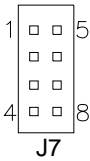
J6: USB6/USB7 Connector

The following table shows the pin outs of the USB pin header.



Signal Name	Pin	Pin	Signal Name
Vcc	1	5	Ground
USB0-	2	6	USB1+
USB0+	3	7	USB1-
Ground	4	8	Vcc

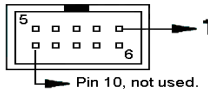
J7: USB4/USB5 Connector



Signal Name	Pin	Pin	Signal Name
Vcc	1	5	Ground
USB0-	2	6	USB1+
USB0+	3	7	USB1-
Ground	4	8	Vcc

J8, J10: COM3, COM4 Serial Ports(RS232)

J8 and J10 are COM pin-header connectors.



Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

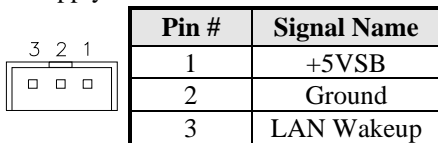
J9: CD-In Audio Connector



Pin #	Signal Name
1	CD Audio R
2	Ground
3	Ground
4	CD Audio L

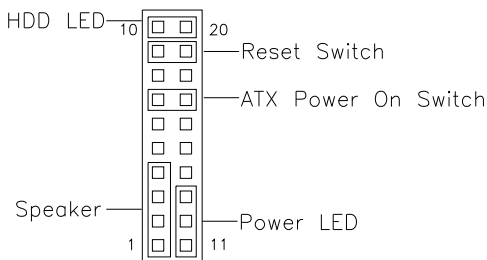
J11: Wake On LAN Connector

J11 is a 3-pin header for the Wake On LAN function on the motherboard. The following table shows the pin out assignments of this connector. Wake On LAN will function properly only with an ATX power supply with 5VSB that has 1A.



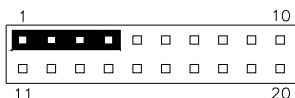
J12: System Function Connector

J12 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status.



Speaker: Pins 1 - 4

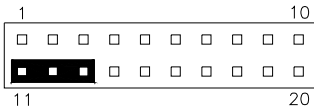
This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.



Pin #	Signal Name
1	Speaker out
2	No connect
3	Ground
4	+5V

Power LED: Pins 11 - 13

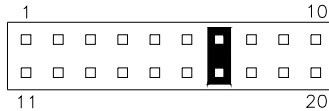
The power LED indicates the status of the main power switch.



Pin #	Signal Name
11	Power LED
12	No connect
13	Ground

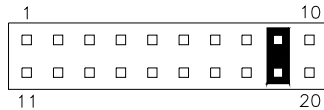
ATX Power ON Switch: Pins 7 and 17

This 2-pin connector is an “ATX Power Supply On/Off Switch” on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.



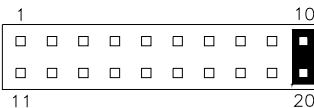
Reset Switch: Pins 9 and 19

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.



Hard Disk Drive LED Connector: Pins 10 and 20

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

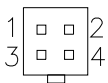


Pin #	Signal Name
10	HDD Active
20	5V

J13: ISA Slot

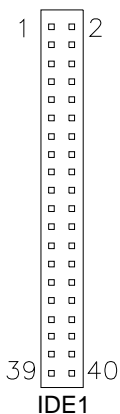
ISA slot does not support ISA master & DMA access function, but only ISA peripheral cards.

JP11: SPDIFI/ SPDIFO Connector (Reserved)



Pin #	Signal Name
1	SPDIF/I
2	Ground
3	SPDIF/O
4	Ground

IDE1: Primary IDE Connectors

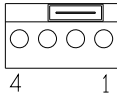


Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Protect pin
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground

Note: The CompactFlash interface cannot be used simultaneously with the IDE interface.

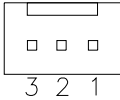
The IDE connector on board does not support OS installation in hard drive. A system hard drive connected to this IDE cannot be booted up to OS.

CPU_FAN1: CPU Fan Power Connector



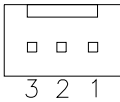
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

SYS_FAN1: system Fan1 Power Connector



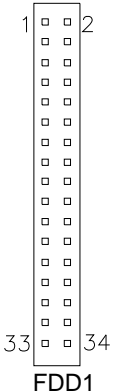
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

SYS_FAN2: SYSTEM Fan2 Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

FDD1: Floppy Drive Connector



Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	RM/LC
Ground	3	4	No connect
Ground	5	6	No connect
Ground	7	8	Index
Ground	9	10	Motor enable 0
Ground	11	12	Drive select 1
Ground	13	14	Drive select 0
Ground	15	16	Motor enable 1
Ground	17	18	Direction
Ground	19	20	Step
Ground	21	22	Write data
Ground	23	24	Write gate
Ground	25	26	Track 00
Ground	27	28	Write protect
Ground	29	30	Read data
Ground	31	32	Side 1 select
Ground	33	34	Diskette change

PCIE_1: x16 PCI Express Slot

PCIE_2: x1 PCI Express Slots

PCI1, PCI2, PCI3, PCI4: PCI Slots

Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=====
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
====
#include <stdio.h>
#include <stdlib.h>
#include "W627EHF.H"
//=====
====
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=====
====
int main (int argc, char *argv[])
{
    unsigned char bBuf;
    unsigned char bTime;
    char **endptr;

    copyright();

    if (argc != 2)
    {
        printf(" Parameter incorrect!!\n");
        return 1;
    }

    if (Init_W627EHF() == 0)
    {
        printf(" Winbond 83627HF is not detected, program abort.\n");
        return 1;
    }
    bTime = strtol (argv[1], endptr, 10);
```



```

    printf("System will reset after %d seconds\n", bTime);

    EnableWDT(bTime);

    return 0;
}
//=====
void copyright(void)
{
    printf("\n===== Winbond 83627EHF Watch Timer Tester (AUTO DETECT)
=====\\n\\
        \" Usage : W627E_WD reset_time\\n\\
        \" Ex : W627E_WD 3 => reset system after 3 second\\n\\
        \" W627E_WD 0 => disable watch dog timer\\n\");
}
//=====
void EnableWDT(int interval)
{
    unsigned char bBuf;

    bBuf = Get_W627EHF_Reg( 0x2D);
    bBuf &= (!0x01);
    Set_W627EHF_Reg( 0x2D, bBuf); //Enable WDTO

    Set_W627EHF_LD( 0x08); //switch to logic device 8
    Set_W627EHF_Reg( 0x30, 0x01); //enable timer

    bBuf = Get_W627EHF_Reg( 0xF5);
    bBuf &= (!0x08);
    Set_W627EHF_Reg( 0xF5, bBuf); //count mode is second

    Set_W627EHF_Reg( 0xF6, interval); //set timer
}
//=====
void DisableWDT(void)
{
    Set_W627EHF_LD(0x08); //switch to logic device 8
    Set_W627EHF_Reg(0xF6, 0x00); //clear watchdog timer
    Set_W627EHF_Reg(0x30, 0x00); //watchdog disabled
}
//=====

```

```

//=====
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
=====
#include "W627EHF.H"
#include <dos.h>
//=====
=====
unsigned int W627EHF_BASE;
void Unlock_W627EHF (void);
void Lock_W627EHF (void);
//=====
unsigned int Init_W627EHF(void)
{
    unsigned int result;
    unsigned char ucDid;

    W627EHF_BASE = 0x2E;
    result = W627EHF_BASE;

    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {    goto Init_Finish; }

    W627EHF_BASE = 0x4E;
    result = W627EHF_BASE;
    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {    goto Init_Finish; }

    W627EHF_BASE = 0x00;
    result = W627EHF_BASE;

Init_Finish:
    return (result);
}
//=====
void Unlock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
}
//=====
=====
void Lock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_LOCK);
}
//=====
void Set_W627EHF_LD (unsigned char LD)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, W627EHF_REG_LD);
    outportb(W627EHF_DATA_PORT, LD);
}

```

```

    Lock_W627EHF();
}
//=====
void Set_W627EHF_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    outportb(W627EHF_DATA_PORT, DATA);
    Lock_W627EHF();
}
//=====
unsigned char Get_W627EHF_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    Result = inportb(W627EHF_DATA_PORT);
    Lock_W627EHF();
    return Result;
}
//=====

//=====
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
#ifndef __W627EHF_H
#define __W627EHF_H        1
//=====
#define    W627EHF_INDEX_PORT        (W627EHF_BASE)
#define    W627EHF_DATA_PORT        (W627EHF_BASE+1)
//=====
#define    W627EHF_REG_LD            0x07
//=====
#define W627EHF_UNLOCK            0x87
#define    W627EHF_LOCK            0xAA
//=====
unsigned int Init_W627EHF(void);
void Set_W627EHF_LD( unsigned char);
void Set_W627EHF_Reg( unsigned char, unsigned char);
unsigned char Get_W627EHF_Reg( unsigned char);
//=====
#endif    //__W627EHF_H

```

File of the Main.cpp

```
//=====
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//=====
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "W627HF.H"
//=====
void ClrKbBuf(void);
int main (int argc, char *argv[]);
//=====
int main (int argc, char *argv[])
{
    unsigned char ucDO = 0;           //data for digital output
    unsigned char ucDI;              //data for digital input
    unsigned char ucBuf;

    Set_W627HF_LD( 0x07);            //switch to logic device 7

    Set_W627HF_Reg(0xF1, 0x00);      //clear
    ucDI = Get_W627HF_Reg(0xF1) & 0x0F;

    ClrKbBuf();
    while(1)
    {
        ucDO++;
        Set_W627HF_Reg(0xF1, ((ucDO & 0x0F) << 4));
        ucBuf = Get_W627HF_Reg(0xF1) & 0x0F;
        if (ucBuf != ucDI)
        {
            ucDI = ucBuf;
            printf("Digital I/O Input Changed. Current Data is 0x%X\n",ucDI);
        }

        if (kbhit())
        {
            getch();
            break;
        }
        delay(500);
    }
    return 0;
}
//=====
void ClrKbBuf(void)
{
    while(kbhit())
    {
        getch();
    }
}
//-----
```

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses that also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278h - 27Fh	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0h - 2DFh	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360h - 36Fh	Network Ports
3B0h - 3BFh	Monochrome & Printer adapter
3C0h - 3CFh	EGA adapter
3D0h - 3DFh	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

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