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2808090 **User's Manual**

Nano-ITX Motherboard

Version 1.0

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How to Use This Manual

1.3 Product Specification

- **Main Processor**
  - On board Intel® ATOM™ Z510 (1.1GHz) / Z530 (1.6GHz) processor
  - CPU clock bus: Z530: 533MHz / Z510:400MHz
- **Chipset**
  Intel® System Controller Hub US15W
- **System BIOS**
  AMI BIOS
- **Main Memory**
  One 200-pin DDR2 SODIMM socket supports up to 2GB dual channel 400/533 MHz memory
- **Expansion Interface**
  One PCI-Express x 1slot
- **Serial Port**
  Support one RS232/422/485
- **USB Interface**
  Support six USB (Universal Serial Bus) ports, four on rear I/O and two on board header for internal devices. USB port6 can support USB 2.0 only base on Intel specification.
- **Audio Interface**
  Connector for Mic-In and Line-Out
- **Watch Dog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - General system reset
- **On board VGA**
  Intel® System Controller Hub US15W integrated GMA 500 Graphic device
- **On-board Ethernet LAN**
  One Gigabit Ethernet (10/100/1000 Mbits/sec) LAN ports using Intel® 82574L PCI-Expressx1interface GbE Ethernet Controller
- **High Drive GPIO**
  On-board programmable 8-bit Digital I/O interface
- **Cooling Fans**
  Support one 3-pin power connector for system fan
- **System Monitoring Feature**
  Monitor system temperature and major power sources.
- **Outline Dimension (L x W)**
  120mm(4.72'') x 120mm(4.72'')

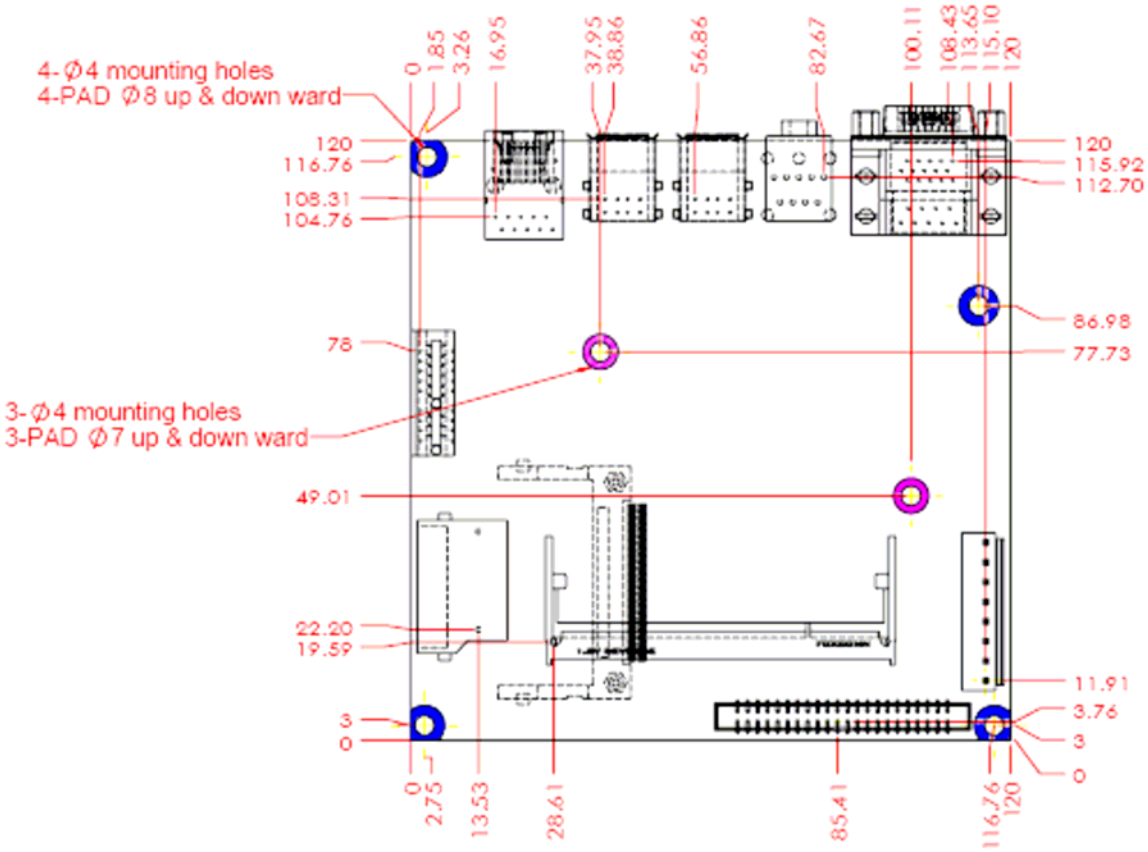
- **Power Requirements**
  Configuration

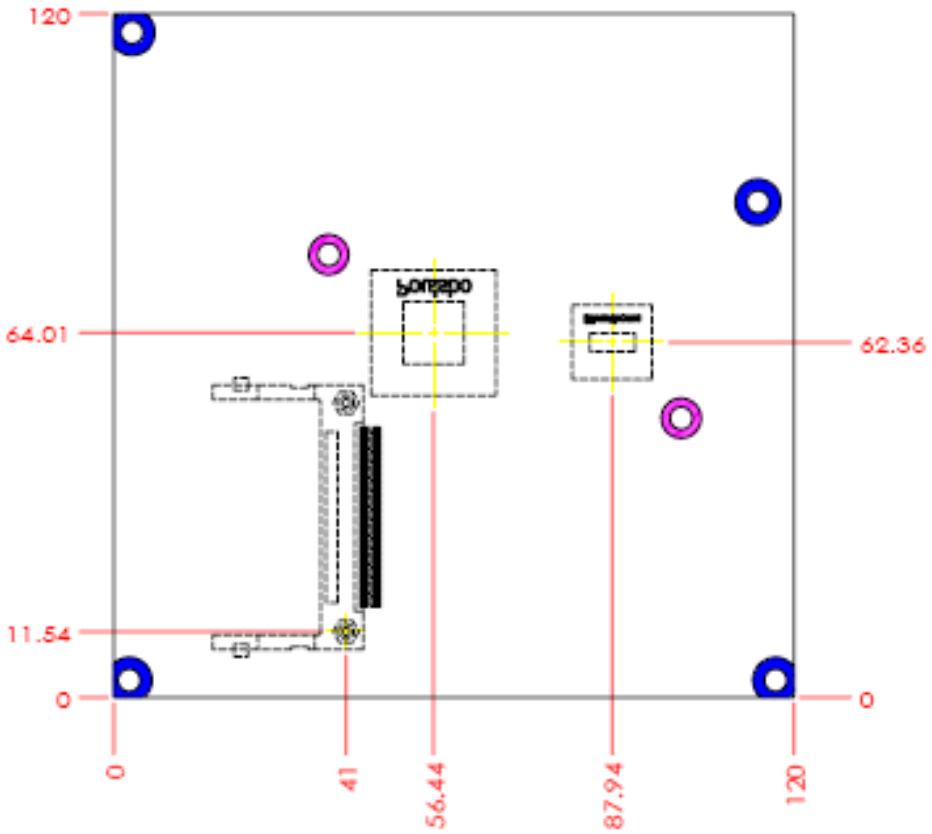
CPU Type	Intel® Atom™ CPU Z510 1.10GHz FSB:400MHz L2:512K
Memory	Apacer DDR2 PC4300 512MB*1 (SAMSUNG K4T51083QE-ZCD5)
VGA Card	Onboard Intel Corporation Poulsbo Embedded Graphics Chipset Function 0
VGA Driver	Intel Corporation Poulsbo Embedded Graphics Chipset Version:9.0.1.1200
LAN Card	Onboard Intel® 82574L Gigabit Network Connection
LAN Driver	Intel® 82574L Gigabit Network Connection Version:10.3.42.0
Audio Card	Onabord Realtek ALC888 High Definition Audio Controller
Audio Driver	Realtek High Definition Audio Controller Version:5.10.0.5296
Chip Driver	Intel® Chipset Device Software Version:8.8.0.1011
USB 2.0 Driver	Intel® SCH Family USB2 Enhanced Host Controller Version:8.8.0.1001
IDE HDD	Seagate ST340014A 40GB
Compact Flash	Apacer AP-CF128B-Steno
CDROM	PIONEER DVD-126A
Power Supply	PW-330ATXE-12V

Item	Power ON	Full Loading 10Min	Full Loading 30Min
System +12V	1.54A	0.38A	0.90A
System +5V	2.04A	2.96A	3.09A

- **Operating Temperature**
  0 °C ~ 60 °C
- **Storage temperature**
  -20 ~ 80 °C
- **Relative Humidity**
  0% ~ 90%, non-condensing

1.3.1 Mechanical Drawing

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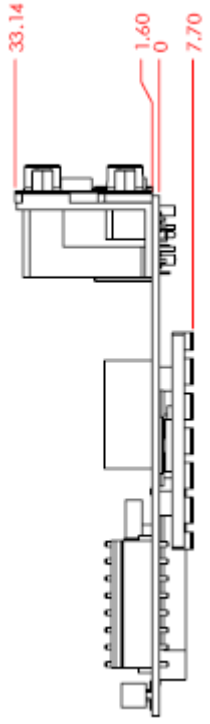
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1.60
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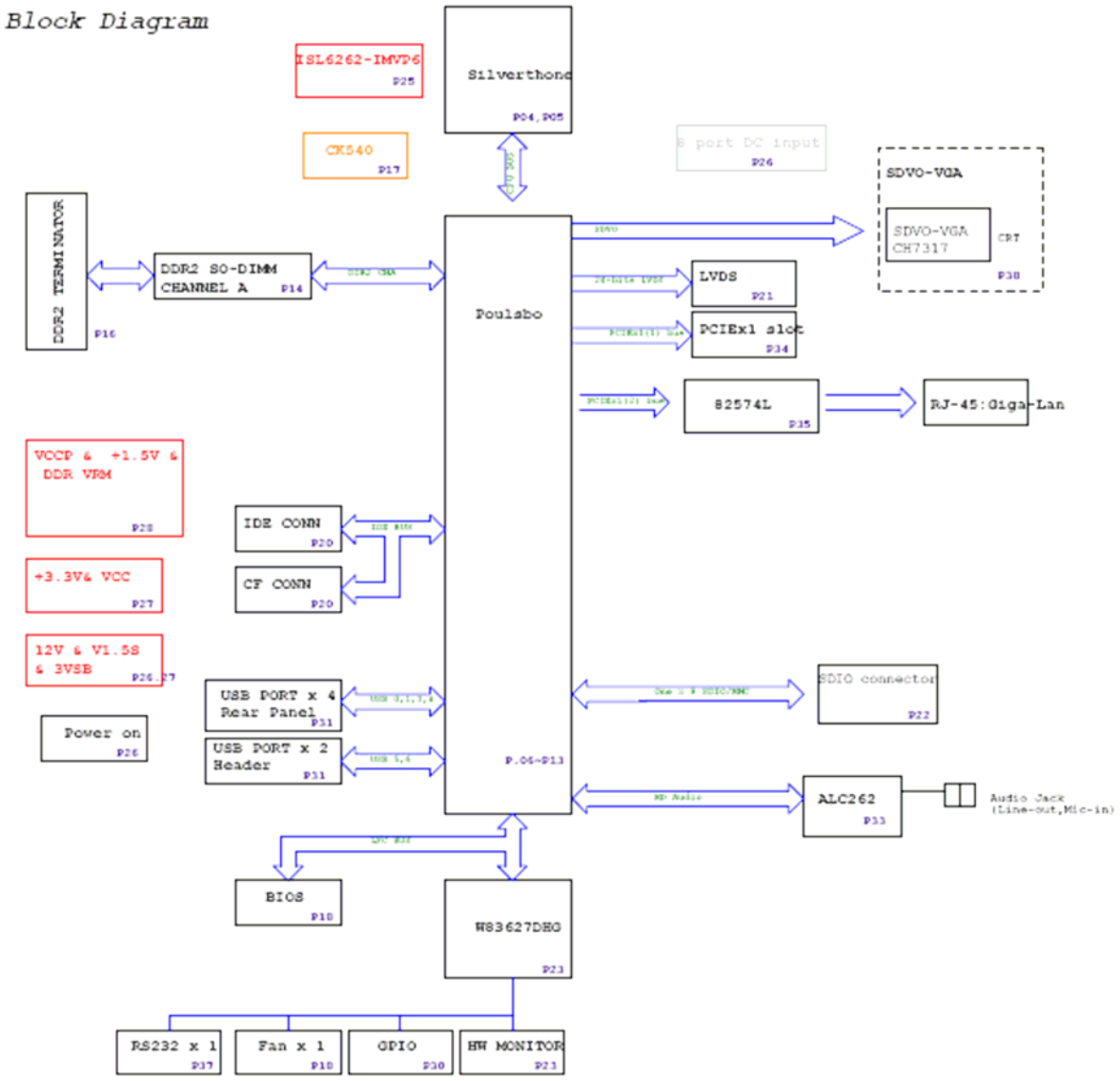
7.70

1.4 System Architecture

All of details operating relations are shown in 2808090 System Block Diagram.



2808090 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on 2808090 are in the proper position. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper allocations.

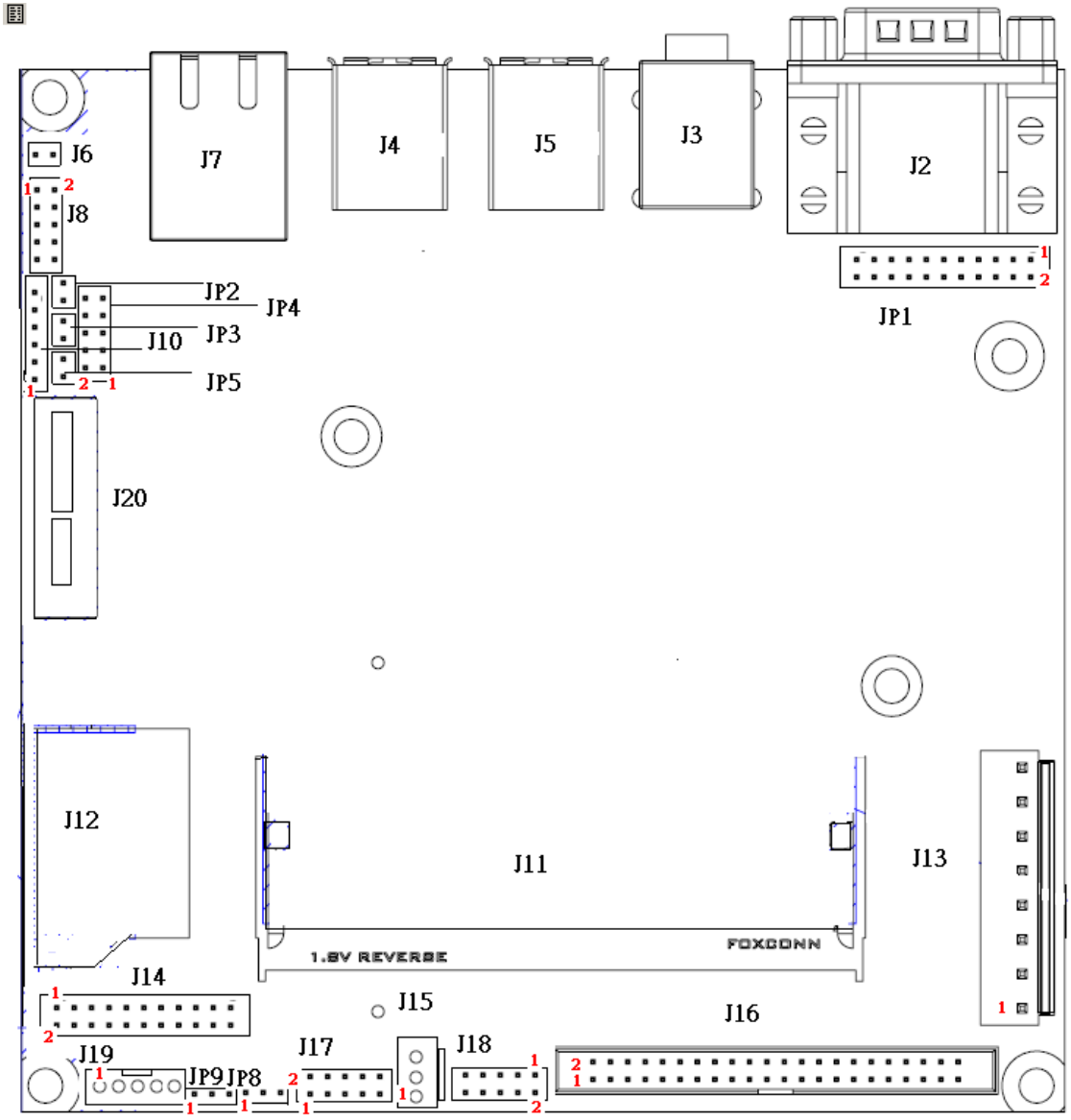


Figure 2-1 2808090 Jumper and Connector Locations

JP9 : 5V / 3.3Vbacklight Inverter Power selection

JP9	Signal Description
1-2 Short	3.3V ★
2-3 Short	5V

JP8 : LCD Power Jump Setting

JP8	Signal Description
1-2 Short	3.3V ★
2-3 Short	5V

JP5 PM_SLPMODE jumper

JP5	Function
1-2 Short	PM_SLPMODE connect

JP3 : SLP_S5 jumper

JP3	Function
1-2 Short	SLP_S5 Enable

JP2 : RSMRST# jumper

JP2	Function
1-2 Short	RSMRST# Enable

JP1 : RS232/422/485 jumper setting

COM Function	Jumper setting
RS-232	5-6,9-11,10-12,15-17,16-18 ★
RS-422	3-4,7-9,8-10,13-15,14-16,21-22
RS-485	1-2,7-9,8-10,19-20

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors

Connector Function List

Connector	Description	Remark
J2	COM+VGA connector	
J3	Audio (LINE_OUT/MIC_IN) Interface connector	
J4/J5	USB connector	
J6	CMOS Clear header	
J7	RJ-45 connector	
J8	Front USB header	
J10	Micro-controller programming header	
J11	DDR2 SO-DIMM	
J12	SD/MMC connector	
J13	Power connector	
J14	LVDS Interface	
J15	Fan header	
J16	Pitch2.0 IDE header	
J17	8-bit GPIO header	
J18	Power button/Reset/HDD LED/SUS LED header	
J19	LVDS inverter header	
J20	PCIEx1 slot	

Pin Assignments of Connectors

J2 : COM+VGA connector

PIN No.	Signal Description	PIN No.	Signal Description
A1	RED	B1	DCD#1/DT1-
A2	Green	B2	RXD#1/DT+
A3	Blue	B3	TXD#1/422R+
A4	NC	B4	DTR#1/422R-
A5	GND	B5	GND
A6	VGA_AL_EN	B6	DSR#
A7	GND	B7	RTS#1
A8	GND	B8	CTS#1
A9	NC	B9	RI#1
A10	GND		
A11	NC		
A12	MONSDA		
A13	MONHSYNC		
A14	MONVSYNC		
A15	MONSCL		

J3 : Audio (LINE_OUT/MIC_IN) Interface connector

PIN No.	Signal Description	PIN No.	Signal Description
Green	LINE_OUT	Pink	MIC_IN

J4/J5 : USB connector

PIN No.	Signal Description	PIN No.	Signal Description
J4	USB port0	J5	USB port3
J4	USB port1	J5	USB port4

J6 : CMOS Clear header

PIN No.	Signal Description
1	RTC_RST#
2	Ground

J7 : RJ45 connector

PIN No.	Signal Description
RJ45	100/Giga network

PIN No.	Signal Description	PIN No.	Signal Description
1	USB0VCC	2	USB0VCC
3	USBD6-	4	USBD5-
5	USBD6+	6	USBD5+
7	USBGND	8	USBGND
9	NC	10	NC

J10 : Micro-controller download firmware header

PIN No.	Signal Description
1	Vpp
2	Vdd
3	Gnd
4	ICSPDAT
5	ICSPCLK
6	NC

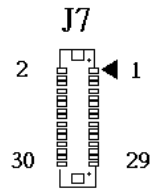
J12 : SDIO/MMC Pin header

PIN No.	Signal Description	PIN No.	Signal Description
1	SLOT_DATA0+	2	+3.3V
3	SLOT_ DATA 1+	4	SLOT_CLK-
5	SLOT_ DATA 2+	6	SLOT_CMD
7	SLOT_ DATA 3+	8	+3.3V
9	SLOT_ DATA 4+	10	GND
11	SLOT_ DATA 5+	12	SLOT_CD#
13	SLOT_ DATA 6+	14	SLOT_WP
15	SLOT_ DATA 7+	16	GND

J13 : Power connector

PIN No.	Signal Description	PIN No.	Signal Description
1	VCC	2	VCC
3	5VSB	4	+12V
5	PS_ON#	6	GND
7	GND	8	GND

J14 : LVDS Interface

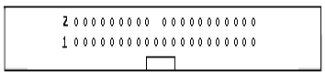


PIN No.	Signal Description	PIN No.	Signal Description
1	Ch1_DATA0+	2	Ch1_ DATA 0-
3	Ch1_ DATA 1+	4	Ch1_ DATA 1-
5	Ch1_ DATA2+	6	Ch1_DATA2-
7	Ch1_ DATA 3+	8	Ch1_ DATA 3-
9	Ch1_ CLK+	10	Ch1_ CLK-
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	L_BKLTCTL	22	NC
23	GND	24	NC
25	GND	26	GND
27	VDD_LVDS	28	VDD_LVDS
29	N/A	30	VDD_LVDS

J15 : Fan header

PIN No.	Signal Description
1	GND
2	FANPWM1
3	FANI01

J16 : 44-pin Hard Disk Connector



PIN No.	Signal Description	PIN No.	Signal Description
1	R_PLT_RST#	2	GND
3	PDD7	4	PDD8
5	PDD6	6	PDD9
7	PDD5	8	PDD10
9	PDD4	10	PDD11
11	PDD3	12	PDD12
13	PDD2	14	PDD13
15	PDD1	16	PDD14
17	PDD0	18	PDD15
19	GND	20	N/C
21	PDDREQ	22	GND
23	PDIOW#	24	GND
25	PDIOR#	26	GND
27	PDIORDY	28	GND
29	PDDACK#	30	GND
31	IRQ14#	32	N/C
33	PDA1	34	GND
35	PDA0	36	PDA2
37	PDCS#1	38	PDCS#3
39	IDEACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C

J17 : 8-bits GPIO header

PIN No.	Signal Description	PIN No.	Signal Description
1	LPC_GP10	2	LPC_GP14
3	LPC_GP11	4	LPC_GP15
5	LPC_GP12	6	LPC_GP16
7	LPC_GP13	8	LPC_GP17
9	GND	10	VCC

J18 : Power button/Reset/HDD LED/SUS LED header

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	PWR_LED
3	5V_Dual	4	SUS_LED
5	VCC3	6	HDD_LED
7	SYS_RESET#	8	GND
9	GND	10	PWR_ON_SW#

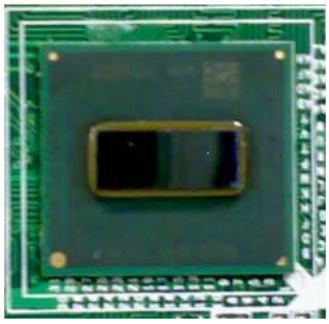
J19 : LCD Panel Power Invert

PIN No.	Signal Description
5	Back light Enable
4	Ground
3	+12V
2	Ground
1	+5V

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel ® ATOM ™ processor Z510/Z530 CPU



Configuring System Bus

2808090 will automatically detect the CPU FSB 400/533MHz CMOS used. CPU speed of Intel ATOM ™ Processor for Mobile can be detected automatically.

3.2 Intel® System Controller Hub US15W

The Intel® System Controller Hub US15W is a low-power chipset in one small 22x22 mm package, It combines the Intel® Graphics Media Accelerator 500, memorycontroller, and I/O controller in a single-chip solution while featuring advanced 3D graphics and extensive I/O capabilities such as USB2.0,SDIO and PCI Express. It supports Intel® High Definition Audio and hardware video decode acceleration, a 400/533 MHz CMOS front-side bus, dual independent display.

3.3 Main Memory

2808090 provides one 200-pin DDR2 SO-DIMM socket which supports 400/533 DDR2-DRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory size can be up to 1GB capacity.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or one single-sided SO-DIMM in socket.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

Memory frequency / CPU FSB synchronization

2808090 supports different memory frequencies depending on the CPU front side bus and the type of DDR2 SO-DIMM.

CPU FSB	Memory Frequency
533MHz	533/400MHz
400 MHz	400MHz

3.4 Installing the Single Board Computer

To install your 2808090 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure memory module on right position
Step 3 : Place the 2808090 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.4.1 to 3.4.4 to install INF/VGA/LAN/Audio drivers.

3.4.1 Chipset Component Driver

The chipset on the 2808090 is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP /VISTA, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in 2808090 CD-title.

3.4.2 Intel Integrated Graphics GMCH Chip

Using Intel® SCH US15W with Media Accelerator High performance graphic integrated chipset is aimed to gain an outstanding graphic performance. Shared 1MB to 8MB system DDR2 SO-DIMM Memory with Total Graphics Memory. This combination makes the 2808090 an excellent piece of multimedia hardware.

Drivers Support

Please find Springdale GMCH driver in the 2808090 CD-title. Drivers support Windows XP / VISTA.

3.4.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find Intel 82574L LAN (J7) drivers in Ethernet directory of 2808090 CD-title. The drivers support Windows XP / VISTA.

LED Indicator (for LAN status)

The 2808090 provides two LED indicators to report Intel 82574L Gigabit Ethernet interface status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">82574L</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><th colspan="2">Linked</th><th>Active</th></tr>
<tr><td>Status LED</td><td>Green</td><td>LAN Linked & Active LED</td><td colspan="2">On</td><td>Blinking</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">LAN speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.4.4 Audio Controller

Please find Realtek ALC888 Audio driver form the 2808090 CD-title. The drivers support Windows XP / VISTA.

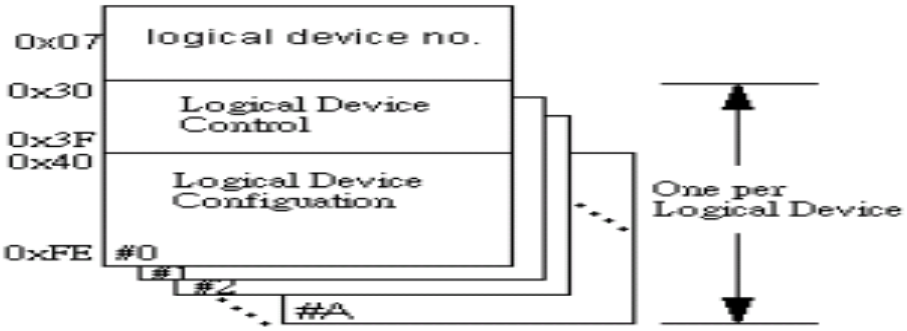
3.5 WDT Function

The algorithm of the WDT function can be simply described as a timer counting process with an output event. The Time-Out period (T_{wd}) can be set by software commands or hardware jumpers that depend on the board circuit design and may be different among the boards. This timer can be used to monitor a software hang.

The 2808090 allows users to control WDT byissuing dynamic software commands. The WDT starts counting when it is activated. It will cause a system reset once it expires. Before WDT expires, a refreshing command with a T_{wd} can be issued to re-count WDT and continue the status monitoring. If the system encounters a software or application hang, WDT will generate a system reset after its timeout.

The related Control Registers of WDT are included in the following programming guide that is written in C language. User can write a non-zero value (defined as T_{wd}) into the Time-out Value Register (CR_T_{wd}) to enable WDT. Users can write 0x00 and then T_{wd} to CR_T_{wd} to refresh WDT. To refresh WDT, the time tolerance of refreshing interval must be considered. The smaller of T_{wd}, the more deviation of WDT and you need to include more tolerance. "Let T_{wd} be longer than 2 seconds" is the recommendation due to the limitation of Winbond W83627DHG WDT. You can call Global support center for reference. The value read back from CR_T_{wd} indicates the counting down value instead of the original T_{wd}. System will be reset after the Time-out Value to be counted down to zero. Users can directly fill a zero value into CR_T_{wd} to disable WDT immediately. To ensure a successful access to the desired Control Register, the following programming guide should be followed.

Programming guide :
CR: Configuration Register.
LD: Logical Device of SIO. There are 11 LDs in W83627DHG SIO.
CR00~2F: Global Control Registers. (All LDs share these CRs)
CR07: LD selection.
CR30~FF: Each LD has its own CR30~FF.



There are two I/O ports as I/O access window for configuring WDT,

1) IO port 0x2E is H/W strapped and named as EFIR (Extended Function Index Register, for identifying CR index number)
2) IO port 0x2F is H/W strapped and named as EFDR (Extended Function Data Register, for accessing desired CR)

<< How to access W83627DHG Configuration Register >>

First, it needs to enter extended function mode.

Enter extended function mode for accessing W83627DHG configuration registers:

```
outportb (EFIR, 0x87);
outportb (EFIR, 0x87);  // double IO write
```

Read Configuration Register CR_rx, and keep this byte to unsigned char al_char

```
outportb(EFIR, CR_rx ) ;
al_char = inportb(EFDR) ;
```

Write Configuration Register CR_wx with byte al_char1 ;

```
outportb (EFIR, CR_wx ) ;
outportb (EFDR, al_char1);
```

Exit extended mode after completion of configuration register access.

```
outportb(EFIR, 0xaa);
```

<< How to access W83627DHG WDT Configuration Register >>

Must enter extended function mode first, then follow the following steps for accessing WDT registers.

Step (1): CR2B_bit4P0

Initialize the multiplex pin (pin89) to WDTO function

```
outportb ( EFIR , 0x2B ) ;          // al_char1 : unsigned char
al_char1 = inportb (EFDR) & 0xEF;  // CR2B_bit4P0
outportb ( EFIR , 0x2B ) ;          // init pin 89 to WDT
outportb ( EFDR , al_char1 ) ;
```

Step (2) : CR07_P08

Ponit to LD8.

```
outportb ( EFIR , 0x07 ) ;
outportb ( EFDR , 0x08 ) ;
```

Step (3) : LD8_CR30_bit0P1

Activate LD8

```
outportb ( EFIR , 0x30 ) ;
al_char1 = inportb ( EFDR ) | 0x01 ;  // CR30_bit0P1
outportb ( EFIR , 0x30 ) ;          // Activate LD8
outportb ( EFDR , al_char1 ) ;
```

Step (4) : LD8_CRF7_bit[7,6]P[0,0]

Not allow K/B and Mouse's interrupts to reload WDT timer.

```
outportb ( EFIR , 0xF7 ) ;
al_char1 = inportb ( EFDR ) & 0x3F ;  // CRF7_bit[7,6]P[0,0]
outportb ( EFIR , 0xF7 ) ;
outportb ( EFDR , al_char1 ) ;
```

Step (5) : Refresh WDT before it expires.

Once WDT expires, system will be reset.

LD8_CRF5_bit3 : 0 : second unit

1: minute unit

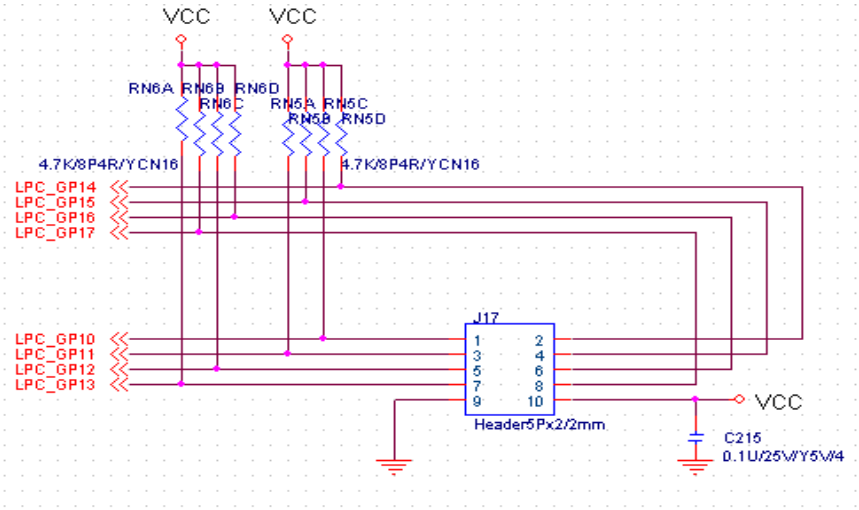
LD8_CRF6: T_{wd} , "Writing 00" means "disable WDT"

1~255 time unit (time unit: second, minute)

Notes:

"CR2B_bit4P0"means " Write 0 to bit4 of Configuration Register 0x2B".

3.6 GPIO



J17 : General Purpose Input/Output Interface Connector

There are 8 GPIO pins on the 2808090.GP10, GP11, GP12 and GP13 are dedicated GPO pins with 12mA current sink capacity at 5V signal level. The output signals have internal weak pull-high resistor, 4.7K Ohm, to 5V.The GPO signals are driven by W83627DHG GP30 ~ 33 pins.

GP14, GP15, GP16 and GP17 are dedicated GPI pins. They are first inverted and then connected to W83627DHG GP34~37 pins.

Refer to the W83627DHG data sheet to configure both input / output port , SGP30~37, by programming W83627DHG GPIO registers. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 =output, 1 = input). Invert port value by setting inversion register (0 = non -inverse, 1 = inverse). Port value is read / written through data register.
In addition, only GP30, GP31 and GP35 are designed to be able to assert PSOUT# or PME# signal to wake up the system if any of them has any transitions. There are about 16mS debounced circuit inside these 3 GPIOs and it can be disabled by programming respective bit (LD9, CR[FEh] bit 4~6).

3.6.1 Pin assignment

J17 : General Purpose I/O Connector

PIN No.	Signal Description
1	General Purpose Input Port 10
2	General Purpose Output Port 14
3	General Purpose Input Port 11
4	General Purpose Output Port 15
5	General Purpose Input Port 12
6	General Purpose Output Port 16
7	General Purpose Input Port 13
8	General Purpose Output Port 17
9	Ground
10	+5V

Programming Guide :
Must enter extended function mode (Double I/O write 0x87 to EFIR) first , then follow the following steps for accessing GPIO pins . When completion of GPIO access, Exit extended mode (I/O write 0xaa to EFIR).

```
void enter_Superio_CFG(void)
{
outportb(Superio_Addr, 0x87);
outportb(Superio_Addr, 0x87);
}
void exit_Superio_CFG(void)
{
outportb(Superio_Addr, 0xAA);
}
```

(1) Initialize W83627DHG multiplex pins to SGP32~34 function

```
enter_Superio_CFG();
   d = GET_CFG(0x2A);
   d = d & 0xFD;
   Set_CFG(0x2A, d);       //  Pin 89,90 function selected by CR2C
   d = GET_CFG(0x2C);
   d = d & 0x1F;
   Set_CFG(0x2C, d);       // Declare Pin88,89,90 as GPIO function
```

(2) Point to LD9 (for SGP30~37 GPIO port registers) and activate its function

```
Set_CFG(0x07, 0x09);          // Select logic device 09
   d = GET_CFG(0x30);
   d = d | 0x02;
   Set_CFG(0x30, d);             //Enable GPIO3
   Set_CFG(0xFE, 0x77);       //Declare GP30,GP31,GP35's triggle type is level and
//diable input de-bouncer
   Set_CFG(0xF2, 0x00);     //Declare GP30~37 without data inversion
```

(3) LD9_CRF0_PF0 ; Set SGP30~33 as GPO pins and SGP34~37 as GPI pin.

```
Set_CFG(0xF0, 0xF0);     //GP30~33 as output;GP34~GP37 as input
```

LD9_CRF1 ; Data Register for reading/writing data to GPIO pins

```
        ; E.g. if put four jumper caps on J17 pin1-2,3-4,5-6,and 7-8
        ; ( Warning : J17 pin9-10 is not allowed to be short circuit. )
        ; and then Write [1,0,1,0] to bit[3:0] , you can get [1,0,1,0] from
        ; bit[7:4].
Set_CFG(0xF1, 0x0A);     //GP30~33 output H,L,H,L
d = GET_CFG(0xF1) & 0xF0;
```

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