integration with integrity

2808180 User's Manual

Intel Core 2 Duo/ GM45 Mini-ITX Motherboard

Version 1.0

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IMPORTANT NOTE: When the system boots without the CRT being connected, there will be no image on screen when you insert the CRT/VGA cable. To show the image on screen, the hotkey must be pressed (CTRL-ALT-F1).

Remarks**: **The IDE connector on board does not support OS installation in hard drive. A system hard drive connected to this IDE cannot be booted up to OS.

Introduction

Product Description

The 2808180 Mini ITX board incorporates the Mobile Intel® GM45 Express Chipset for Embedded Computing, consisting of the Intel® GM45 Graphic Memory Controller Hub (GMCH) and Intel® I/O Controller Hub (ICH9-M), an optimized integrated graphics solution with a 1066MHz and 800MHz front-side bus. Dimensions of the board are 170mm x 170mm.

The integrated powerful 3D graphics engine, based on Intel® Graphics Media Accelerator X3500 (Intel® GMA X3500) architecture, operates at core speeds of up to 533 MHz. It features a low-power design, is validated with the Intel® Core 2 Duo processors on 45nm process. With dual channel DDR2 800MHz two SoDIMM sockets on board, the board supports up to 4GB of DDR2 system memory.

Intel® Graphics supports a unique intelligent memory management scheme called Dynamic Video Memory Technology (DVMT). DVMT handles diverse applications by providing the maximum (384MB) availability of system memory for general computer usage, while supplying additional graphics memory when a 3D-intensive application requests it. The Intel GMA X3500 graphics architecture also takes advantage of the high-performance Intel processor. Intel GMA X3500 graphics supports Dual Independent Display technology.

The main features of the board are:

- Supports Intel® Core™ 2 Duo (Penryn 1066MHz)
- Supports up to 2.53GHz, 1066MHz/800MHz FSB
- Two DDR2 SoDIMM, Max. 4GB memory
- Onboard Gigabit PHY and Intel PCI-Express Gigabit LAN
- Intel® GM45 Express VGA for CRT / LVDS
- 4x SATA, 8x USB 2.0, 4x COM, Watchdog timer
- 1x Mini PCI-E (Mini Card), 1x PCI, 1xPCI-E(x1) slots

Optional daughter cards:

3901080: Chrontel 7308, supports 24 bit single or dual LVDS channel

3901220: Chrontel 7021, supports CRT

3901100: Chrontel 7307C, single DVI (connector on cable)

3901090: Chrontel 7307C, dual DVI (connector on cable)

3901180: Chrontel 7307C, dual DVI (one connector on card and one on cable)

Checklist

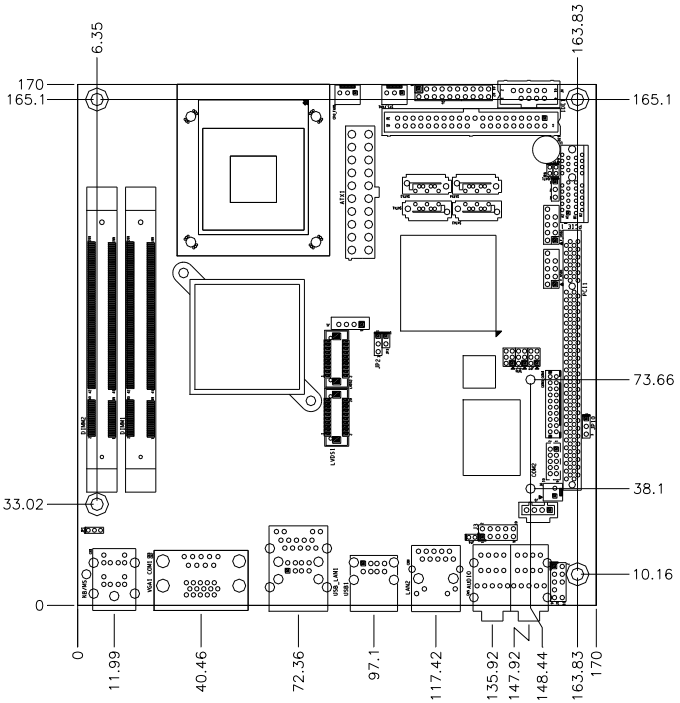
Your 2808180 package should include the items listed below.

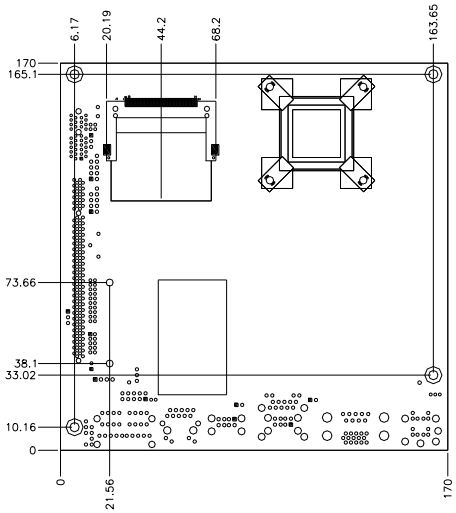
- The 2808180 Mini-ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Cable kit (IDE, Serial port, Serial ATA)

2808180 Specifications

CPU Supported	Intel® Core™ 2 Duo (Penryn), mobile processors
CPU Voltage	0.700V ~ 1.5V (IMVP-6)
System Speed	Up to 2.53GHz or above
CPU FSB	667MHz/800MHz/1066MHz FSB
Cache	1MB/2MB/4MB
Green /APM	APM1.2
CPU Socket	mPGA Socket 478
Chipset	Intel GM45 Chipset GMCH: GM45 1329-pin Micro-FCBGA ICH9M: 82801IBM 678-pin mBGA
BIOS	Award BIOS, supports ACPI function
Memory	DDR2 667/800 SoDIMM x2 (w/o ECC function), Max. 4GB
VGA	GM45 built-in, supports CRT
SDVO (Dual CH)	Through 3901080 card (Chrontel 7308, 24+24 bits single/dual channel LVDS, Chrontel 7021, CRT) Through 3901100 card (Chrontel 7307C, DVI single or Dual)
LVDS LCD Panel	GM45 built-in, supports 24-bit, single or dual channel LVDS
LAN	1. ICH9M 10/100/gigabit MAC + PHY • Intel 82567L 10/100/1000 2. Intell 82574L PCI-e Gigabit LAN controller x1 (2808180A)
USB	ICH9M built-in USB 2.0 host controller, support 8 ports
Serial ATA Ports	ICH9M built-in SATA controller, supports 4 ports
TPM1.2	ICH9M built-in iTPM version1.2 controller by firmware implement
Parallel IDE	JMicron JM368 (PCI-e to PATA) x1 for 1 PATA channel for IDE & CF
Audio	ICH9M built-in audio controller + AC97 Codec ALC888 w/ 7.1 channels, SPDIF-OUT
LPC I/O	W83627DHG: COM1, COM2 (RS232/RS422/RS485), hardware monitor (3 thermal, 4 voltage monitor inputs, 2 fan headers) - Fintek 81216G for COM3 and COM4
Digital IO	4 in & 4 out
Keyboard/Mouse	Supports PS/2 keyboard/mouse connector
Expansion Slots	PCI slot x1, PIC-E (x1) slot x1 and Mini PCIE socket x1
Edge Connector	PS/2 connector x1 for keyboard/mouse Gigabit LAN RJ-45 + dual USB stack connector Gigabit LAN RJ45 Dual USB stack connector DB9 x1 for COM 1; DB15 x1 for VGA RCA Jack 3x2 for Audio (Front-Out, Line-In, Mic, Center/LFE, Surround & Surround Back)
Onboard Header/ Connector	40 pins box-header x1 for IDE1 CF connector x1 @ solder side 10-pin headerx1 for Digital I/O; 10-pin header x1 for COM2 10-pin header x 2 for USB 5,6;7,8 DF13 connector x2 for LVDS; 10-pin header x1 for audio Line-Out & Mic 4-pin header x1 for CD in, SPDIF-out connector x1 SATA connector x4 for SATA ports
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	+5V, +3.3V, +12V, -12V, 5VSB (2A)
Others	Modem Wakeup, LAN Wakeup
Board Size	170mm x 170mm (Mini ITX)

Board Dimensions



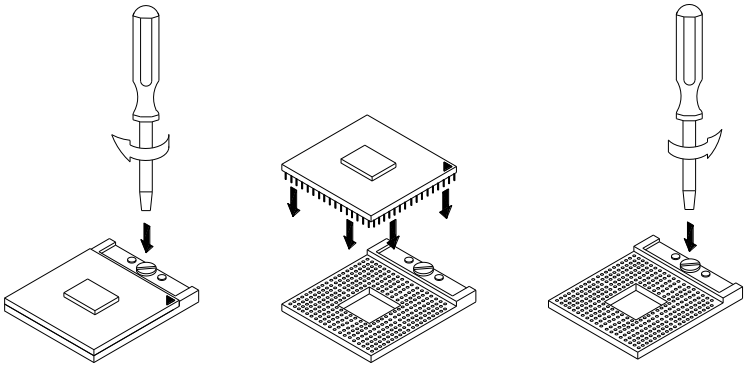


Installations

This section provides information on how to use the jumpers and connectors on the 2808180 in order to set up a workable system. The topics covered are:

Installing the CPU

The 2808180 with socket P
for Intel® Core™ 2 Duo, Intel® Celeron 5 x 5 series processors.
The processor socket comes with a screw to secure the processor. As shown in the left picture below, loosen the screw first before inserting the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, fasten the screw. Refer to the figures below.



NOTE: *Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

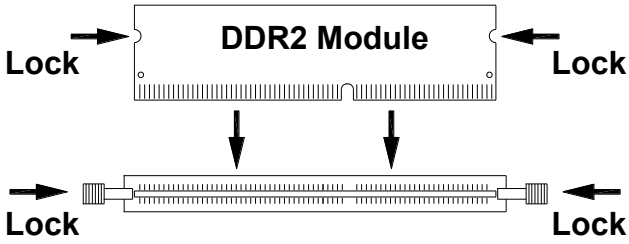
Installing the Memory

The 2808180 board supports two DDR2 memory socket for a maximum total memory of 4GB in DDR2 memory type.

Installing and Removing Memory Modules

To install the DDR2 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR2 module so that the key of the DDR2 module aligned with that on the memory slot.
2. Gently push the DDR2 module in an upright position until the clips of the slot close to hold the DDR2 module in place when the DDR2 module touches the bottom of the slot.
3. To remove the DDR2 module, press the clips with both hands.



Setting the Jumpers

Jumpers are used on 2808180 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on 2808180 and their respective functions.

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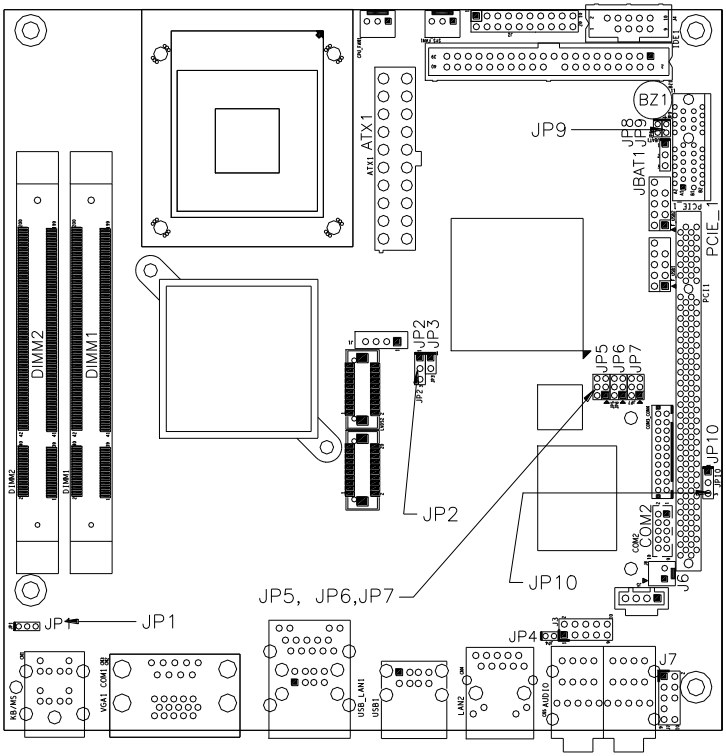
Jumper Locations on 2808180



JP1: Keyboard/Mouse Power Selection

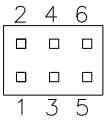
JP1	KB/MS Power
	5V
	5VSB(Standby)

JP2: LCD Panel Power Selection

JP2	LCD Panel Power
	3.3V
	5V

JP5, JP6, JP7: RS232/422/485 (COM2) Selection

COM1 is fixed for RS-232 use only.
COM2 is selectable for RS232, RS-422 and RS-485.
The following table describes the jumper settings for COM2 selection.



COM2 Function	RS-232	RS-422	RS-485
Jumper Setting (pin closed)	JP5: 1-2 JP6: 3-5 & 4-6 JP7: 3-5 & 4-6	JP5: 3-4 JP6: 1-3 & 2-4 JP7: 1-3 & 2-4	JP5: 5-6 JP6: 1-3 & 2-4 JP7: 1-3 & 2-4

COM2 is jumper selectable for RS-232, RS-422 and RS-485.

Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	RTS-	NC
7	RTS	RTS+	NC
8	CTS	CTS+	NC
9	RI	CTS-	NC
10	NC	NC	NC

JP9: CompactFlash Slave/Master Selection

JP9	CF Setting
	Master
	Slave

JP10: PCI/PCIE Riser Card Selection

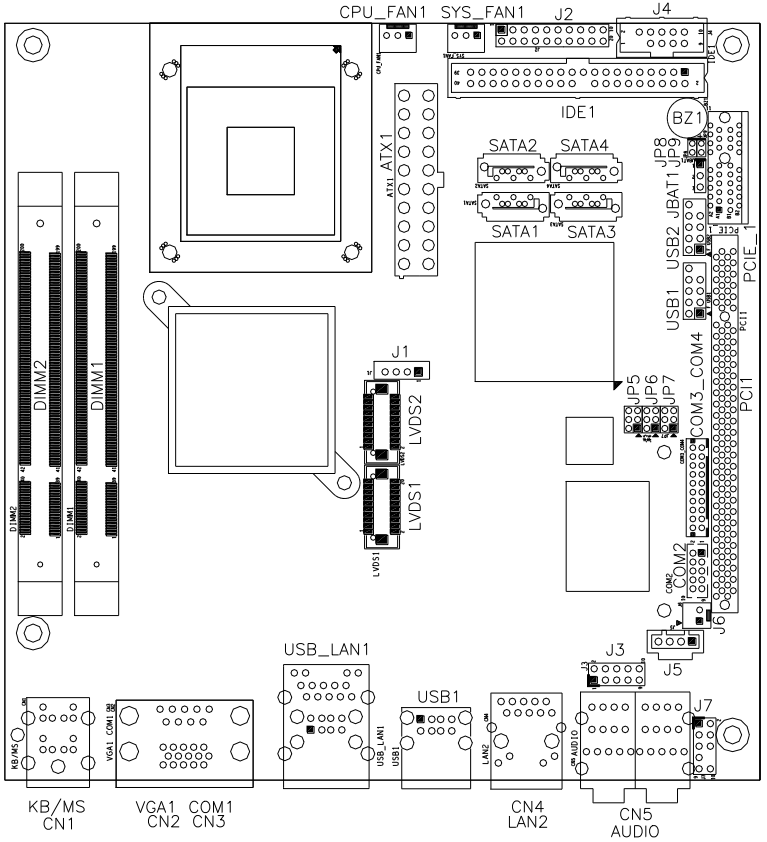
JP10	Riser Card
	IP390 Riser Card Install
	IP151, IP240 Riser Card Install

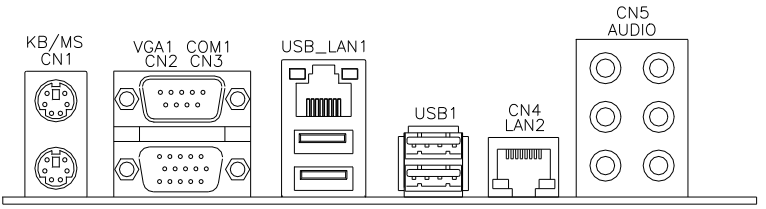
JBAT1: Clear CMOS Setting

JBAT1	Setting
	Normal
	Clear CMOS

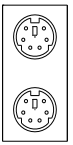
Connectors on 2808180

Connector Locations on 2808180





CN1: PS/2 Keyboard and PS/2 Mouse Connectors

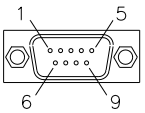


PS/2 Mouse

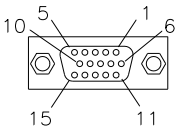
PS/2 Keyboard

Signal Name	Keyboard	Mouse	Signal Name
Keyboard data	1	1	Mouse data
N.C.	2	2	N.C.
GND	3	3	GND
5V	4	4	5V
Keyboard clock	5	5	Mouse clock
N.C.	6	6	N.C.

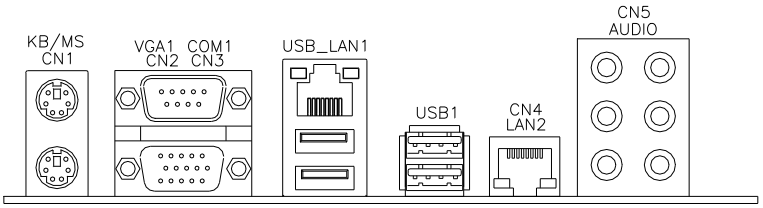
CN2, CN3: COM1 and VGA Connector



Signal Name	Pin #	Pin #	Signal Name
DCD	1	6	DSR
RXD	2	7	RTS
TXD	3	8	CTS
DTR	4	9	RI
GND	5	10	Not Used



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
N.C.	9	10	GND
N.C.	11	12	N.C.
HSYNC	13	14	VSYNC
NC	15		



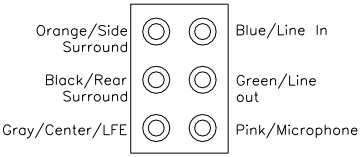
USB_LAN1: 10/100/1000 RJ-45 (2808180) and USB1/2 Ports

CN4: GbE RJ-45 (2808180A)

USB1: USB3/4 Ports

J6: SPDIF Out Connector

CN5: Audio Connector



SYS_FAN1: System Fan Power Connector

This is a 3-pin header for system fans. The fan must be a 12V (500mA).

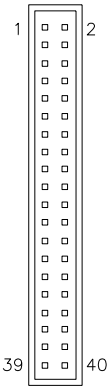
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

CPU_FAN1: CPU Fan Power Connector

This is a 3-pin header for the CPU fan. The fan must be a 12V fan.

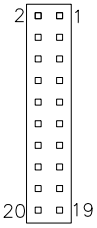
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

IDE1: IDE Connector



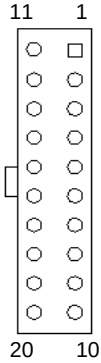
Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Protect pin
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground

COM3_COM4: COM3, COM4 Serial Port



Signal Name	Pin #	Pin #	Signal Name
DSR	2	1	DCD
RTS	4	3	RXD
CTS	6	5	TXD
RI	8	7	DTR
NA	10	9	Ground
DSR	12	11	DCD
RTS	14	13	RXD
CTS	16	15	TXD
RI	18	17	DTR
NA	20	19	Ground

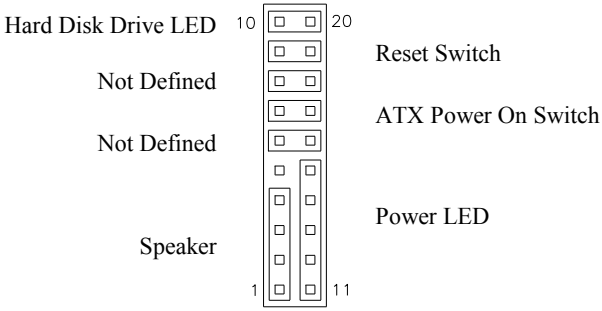
ATX1: ATX Power Supply Connector



Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

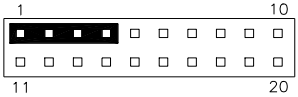
J2 (F_PANEL): System Function Connector

J2 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J2 is a 20-pin header that provides interfaces for the following functions.



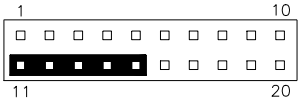
Speaker: Pins 1 - 4

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.



Pin #	Signal Name
1	Speaker out
2	No connect
3	Ground
4	+5V

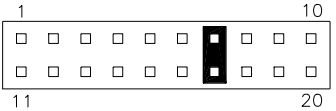
Power LED: Pins 11 - 15



Pin #	Signal Name
11	Power LED
12	No connect
13	Ground
14	No connect
15	Ground

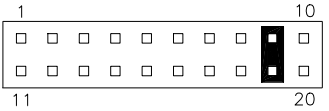
ATX Power ON Switch: Pins 7 and 17

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.



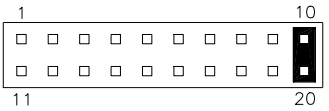
Reset Switch: Pins 9 and 19

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.



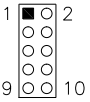
Hard Disk Drive LED Connector: Pins 10 and 20

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.



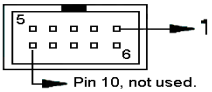
Pin #	Signal Name
10	HDD Active
20	5V

F_USB1: USB5/USB6 Connector



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Vcc
D0-	3	4	D1-
D0+	5	6	D1+
Ground	7	8	Ground
NC	9	10	Ground

COM2: COM2 Serial Port

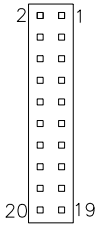


COM2

Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

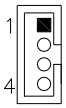
LVDS1, LVDS2: LVDS Connectors (1st channel, 2nd channel)

The LVDS connectors on board consist of the first channel (LVDS1) and second channel (LVDS2).



Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

J1: LCD Backlight Connector

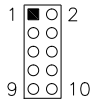


Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

JMINI: Mini PCIE Connector

SATA1, SATA2, SATA3, SATA4: SATA Connectors

J3: Digital I/O



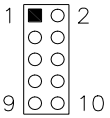
Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J5: CD-In Pin Header

Pin #	Signal Name
1	CD Audio R
2	Ground
3	Ground
4	CD Audio L

J4: SPI Flash Connector (factory use only)

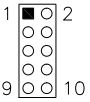
J7: Front Audio Connector



Signal Name	Pin #	Pin #	Signal Name
MIC2_L	1	2	Ground
MIC2_R	3	4	Presence#
Line2_L	5	6	MIC2_ID
Sense	7	8	NC
Line2_R	9	10	Line2_ID

J8: PCI-E(x1) Slot

F_USB2: USB7/USB8 Connector



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Vcc
D0-	3	4	D1-
D0+	5	6	D1+
Ground	7	8	Ground
NC	9	10	Ground

J9: Compact Flash Connector

PCI1: PCI Slot (supports 2 Master)

CON1: SDVO Port Connector

Signal Name	Pin #	Pin #	Signal Name
+12V	A1	B1	+12V
+12V	A2	B2	+12V
+5V	A3	B3	+5V
3.3V	A4	B4	3.3V
RESET	A5	B5	GND
GND	A6	B6	GND
SDVOC_CLK+	A7	B7	SDVOC_CLK-
SDVOC_Blue+	A8	B8	SDVOC_Blue-
GND	A9	B9	GND
SDVOC_Green+	A10	B10	SDVOC_Green-
SDVOC_Red+	A11	B11	SDVOC_Red-
GND	A12	B12	GND
SDVO TVClkIn+	A13	B13	SDVO TVClkIn-
SDVOB Int+	A14	B14	SDVOB Int-
GND	A15	B15	GND
SDVO CtrlData	A16	B16	SDVO CtrlClk
SDVOB Clk+	A17	B17	SDVOB Clk-
GND	A18	B18	GND
SDVOB Blue+	A19	B19	SDVOB Blue-
SDVOB Green+	A20	B20	SDVOB Green-
GND	A21	B21	GND
SDVOB Red+	A22	B22	SDVOB Red-
SDVO Stall+	A23	B23	SDVO Stall-
GND	A24	B24	GND

Headers and Connectors on 2808180

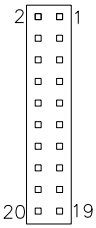
3901080 – JP4 LCD Panel Power Selection

JP4	Voltage
	3.3V
	5V

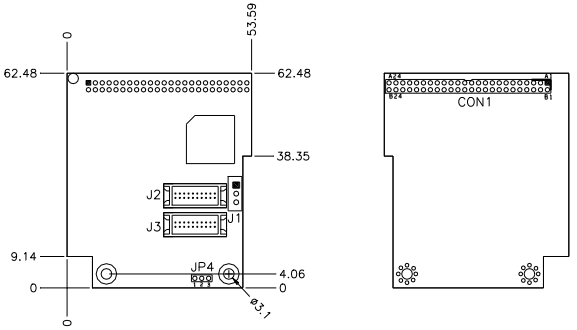
3901080 – J1 LCD Backlight Setting

Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Ground

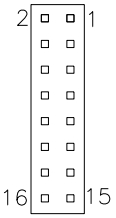
3901080 – J3 and J2 1st/2nd LVDS Channel Connectors



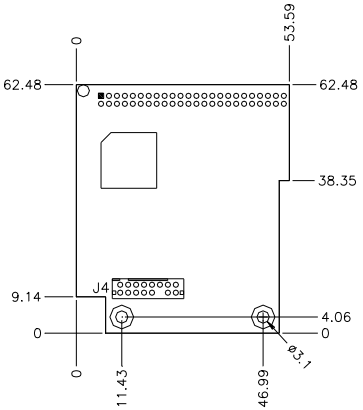
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V



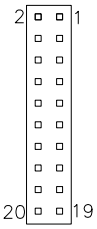
3901220 – J4 VGA Connector



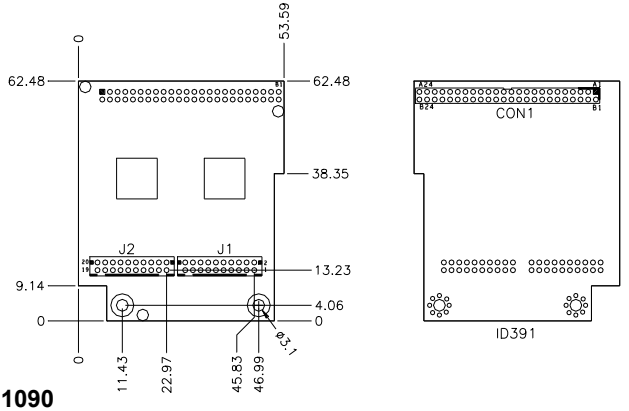
Signal Name	Pin #	Pin #	Signal Name
+5V	2	1	RED
Ground	4	3	GREEN
N.C.	6	5	BLUE
SDA	8	7	N.C.
HSYNC	10	9	Ground
VSYNC	12	11	Ground
SCL	14	13	Ground
N.C.	16	15	Ground



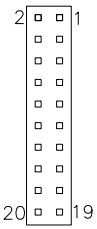
3901100 – J2 DVI Connector



Signal Name	Pin #	Pin #	Signal Name
TDC1-	2	1	TDC1+
Ground	4	3	Ground
TLC-	6	5	TLC+
+5V	8	7	Ground
NC	10	9	HPDET
TDC2-	12	11	TDC2+
Ground	14	13	Ground
TDC0-	16	15	TDC0+
NC	18	17	NC
DDC_SC	20	19	DDC_SD



3901090 – J1, J2 1st/2nd DVI Connectors



Signal Name	Pin #	Pin #	Signal Name
TDC1-	2	1	TDC1+
Ground	4	3	Ground
TLC-	6	5	TLC+
+5V	8	7	Ground
NC	10	9	HPDET
TDC2-	12	11	TDC2+
Ground	14	13	Ground
TDC0-	16	15	TDC0+
NC	18	17	NC
DDC_SC	20	19	DDC_SD

Remarks: When using dual DVI, the first DVI video output is through J1. After setting the drivers in Windows, then the second DVI output (via J2) will function. 3901090 and 3901100 are different since the latter (3901100) has video output via J2. The pin assignments of J1 and J2 are the same.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=============================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=============================================================================
#include <stdio.h>
#include <stdlib.h>
#include "W627DHG.H"
//=============================================================================
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=============================================================================
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        copyright();

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return 1;
        }

        if (Init_W627DHG() == 0)
        {
                printf(" Winbond 83627HF is not detected, program abort.\n");
                return 1;
        }
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        EnableWDT(bTime);

        return 0;
}
//=============================================================================
```

```
void copyright(void)
{
        printf("\n========= Winbond 83627DHG Watch Timer Tester (AUTO DETECT) ========\n"\
                        "       Usage : W627E_WD reset_time\n"\
                        "       Ex : W627E_WD 3  => reset system after 3 second\n"\
                        "            W627E_WD 0  => disable watch dog timer\n");
}
//===========================================================================
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_W627DHG_Reg( 0x2D);
        bBuf &= (!0x01);
        Set_W627DHG_Reg( 0x2D, bBuf);                   //Enable WDTO

        Set_W627DHG_LD( 0x08);                          //switch to logic device 8
        Set_W627DHG_Reg( 0x30, 0x01);                   //enable timer

        bBuf = Get_W627DHG_Reg( 0xF5);
        bBuf &= (!0x08);
        Set_W627DHG_Reg( 0xF5, bBuf);                   //count mode is second

        Set_W627DHG_Reg( 0xF6, interval);               //set timer
}
//===========================================================================
void DisableWDT(void)
{
        Set_W627DHG_LD(0x08);                           //switch to logic device 8
        Set_W627DHG_Reg(0xF6, 0x00);                    //clear watchdog timer
        Set_W627DHG_Reg(0x30, 0x00);                    //watchdog disabled
}
//===========================================================================
```

```
//=============================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=============================================================================
#include "W627DHG.H"
#include <dos.h>
//=============================================================================
unsigned int W627DHG_BASE;
void Unlock_W627DHG (void);
void Lock_W627DHG (void);
//=============================================================================
unsigned int Init_W627DHG(void)
{
	unsigned int result;
	unsigned char ucDid;

	W627DHG_BASE = 0x2E;
	result = W627DHG_BASE;

	ucDid = Get_W627DHG_Reg(0x20);
	if (ucDid == 0x88)
	{	goto Init_Finish;	}

	W627DHG_BASE = 0x4E;
	result = W627DHG_BASE;
	ucDid = Get_W627DHG_Reg(0x20);
	if (ucDid == 0x88)
	{	goto Init_Finish;	}

	W627DHG_BASE = 0x00;
	result = W627DHG_BASE;

Init_Finish:
	return (result);
}
//=============================================================================
void Unlock_W627DHG (void)
{
	outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
	outportb(W627DHG_INDEX_PORT, W627DHG_UNLOCK);
}
//=============================================================================
void Lock_W627DHG (void)
{
	outportb(W627DHG_INDEX_PORT, W627DHG_LOCK);
}
//=============================================================================
void Set_W627DHG_LD( unsigned char LD)
{
	Unlock_W627DHG();
	outportb(W627DHG_INDEX_PORT, W627DHG_REG_LD);
	outportb(W627DHG_DATA_PORT, LD);
	Lock_W627DHG();
}
```

```
//=============================================================================
void Set_W627DHG_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_W627DHG();
	outportb(W627DHG_INDEX_PORT, REG);
	outportb(W627DHG_DATA_PORT, DATA);
	Lock_W627DHG();
}
//=============================================================================
unsigned char Get_W627DHG_Reg(unsigned char REG)
{
	unsigned char Result;
	Unlock_W627DHG();
	outportb(W627DHG_INDEX_PORT, REG);
	Result = inportb(W627DHG_DATA_PORT);
	Lock_W627DHG();
	return Result;
}
//=============================================================================
```

```
//=============================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=============================================================================
#ifndef __W627DHG_H
#define __W627DHG_H			1
//=============================================================================
#define W627DHG_INDEX_PORT		(W627DHG_BASE)
#define W627DHG_DATA_PORT		(W627DHG_BASE+1)
//=============================================================================
#define W627DHG_REG_LD			0x07
//=============================================================================
#define W627DHG_UNLOCK			0x87
#define W627DHG_LOCK			0xAA
//=============================================================================
unsigned int Init_W627DHG(void);
void Set_W627DHG_LD( unsigned char);
void Set_W627DHG_Reg( unsigned char, unsigned char);
unsigned char Get_W627DHG_Reg( unsigned char);
//=============================================================================
#endif //__W627DHG_H
```

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