User's Manual

3307246

Manual Objectives

This manual describes in detail the Global American, Inc. 3307246 Embedded System Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with 3307246 or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

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How to Use This Manual

The manual describes how to configure your 3307246 system to meet various operating requirements. It is divided into four chapters, with each chapter addressing a basic concept and operation of Embedded Board Computer.

Chapter 1: Introduction. This chapter presents what you have in the inside of box and give you an overview of the product specifications and basic system architecture for this model of single board computer.

Chapter 2: Hardware Configuration Setting. This chapter shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3: System Installation. This chapter describes how to properly mount the CPU and main memory, M-system Flash disk, or optional flat panel display interface module to get a safe installation and give you a programming guide of Watch Dog Timer function. Besides, it will introduce and show you the driver installation procedure about Graphics Controller.

Chapter 4: BIOS Setup Information. This chapter specifies the meaning of each setup parameters and how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give you a guide of trouble-shooting.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Global American, Inc.** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site: http://www.globalamericaninc.com

EC Declaration of Conformity

(To Be Added)

For the following equipment is herewith confirmed to comply with the requirements set out in the Council Directive on the Approximation of the Laws of the Member States relating to Electromagnetic Compatibility Directive (89/336/EEC). The equipment was evaluated and passed the test, the following standards were applied:

EMC :	EN 55022	(1994/A1:1995 Class A)
	EN 50082-2	(1991)
	EN 61000-4-2	(1995)
	EN 61000-4-3	(1996)
	EN 61000-4-4	(1995)
	EN 61000-3-2	(1995)
	EN 61000-3-3	(1995)

1. Introduction

1.1 System Overview

The 3307246 is a compact 5.25" CD-ROM size Single Board Computer that equips with VIA Apollo Pro 133A AGPset, SMI AGP 2X Lynx3DM 2D/3D Graphics and Multimedia Accelerator w/ Embedded 4MB SGRAM, Dual LCD interfaces, NTSC/PAL TV output, AC97 Audio, and dual PCI-bus Ethernet interfaces.

Targeting on the rapid growing networking and multimedia embedded markets, the 3307246 comes designed with dual PCI-bus Intel 82559ER 10/100Base-Tx chips and dual LCD interfaces. This make it a perfect solution for not only popular Networking Devices like Firewall, Gateway, Router, Thin Server, and E-Box but also Retail / Financial Transaction Terminals, and high-end multimedia POS / KIOSK Terminals.

In addition, the on board 24-bit Panel Link interface, Zoom Video port, and NTSC/PAL TV output interface make the 3307246 also ideal for demanding high-end Entertainment Devices that require high integration multimedia Single Board Computer.

Other impressive features include PC133 FSB, Ultra DMA66 IDE, a Compact Flash socket for type I/II Compact Flash storage card, four serial ports, one parallel port, one 168-pin DIMM socket allowing for up to 256MB of SDRAM to be installed, and a PCI slot for future expansion.

1.2 Check List

- 1 3307246 All-in-One FC370 Celeron / Pentium III Computing Module
- 1 Quick Installation Guide
- 1 CD-ROM contains the followings:
  - User's Manual (this manual in PDF file)
  - Ethernet driver and utilities
  - VGA drivers and utilities
  - Audio drivers and utilities

Latest BIOS (as of the CD-ROM was made)

Introduction

1.3 System Specifications

General Functions

- **CPU:** Intel FC-370 Pentium III/Celeron (with system bus frequencies of 66/100/133MHz)
- **CPU socket:** Intel Socket 370
- **BIOS:** Award 256KB Flash BIOS
- **Chipset:** VIA Apollo Pro 133A, VT82C694X
- **I/O Chipset:** VT82C686A / Winbond W83977EF-AW
- **Memory:** Onboard one 168-pin DIMM socket supports up to 256 Mbytes SDRAM
- **Enhanced IDE:** Supports two IDE devices. Supports Ultra DMA/66 mode with data transfer rate up to 66MB/sec. (20 x 2 header onboard)
- **FDD interface:** Supports up to two floppy disk drives, 5.25" (360KB and 1.2MB) and/or 3.5" (720KB, 1.44MB and 2.88MB)
- **Parallel port:** One bi-directional parallel port. Supports SPP, ECP, and EPP modes
- **Serial port:** Three RS-232 and one RS-232/422/485 serial port. Ports can be configured as COM1, COM2, COM3, COM4, or disabled individually. (16C550 equivalent)
- **IR interface:** Supports one IrDA Tx/Rx header
- **KB/Mouse connector:** 8-pin (4 x 2) connector supports PS/2 keyboard and mouse
- **USB connectors:** One 5 x 2 header onboard supports dual USB ports
- **Watchdog Timer:** Can generate a system reset, IRQ15 or NMI. Software selectable time out interval (32 sec. ~ 254 min., 1 min./step)
- **DMA:** 7 DMA channels (8237 equivalent)
- **Interrupt:** 15 interrupt levels (8259 equivalent)

- **Power management:** Supports ATX power supply. Supports PC97, LAN wake up and modem ring-in functions. I/O peripheral devices support power saving and doze/standby/suspend modes. APM 1.2 compliant.

Flat Panel/CRT Interface

- **Chipset:** SMI Lynx3DM SM721, high performance 128-bit GUI, 3D engine
- **Display memory:** 4 MB of SGRAM frame buffer on Lynx3DM SM721G4. Optional 8 MB SGRAM frame buffer on Lynx3DM SM721G8
- **Display type:** Simultaneously supports CRT and flat panel (EL, LCD and gas plasma) displays
- **Interface:** 2X AGP, Accelerator Graphics Ports 1.0 compliant
- **Display mode:**

  LCD panel supports up to 800 x 600 @ 24 bpp, 1024 x 768 @ 24 bpp

  CRT displays support up to 800 x 600 @ 24 bpp, 1024 x 768 @ 24 bpp
- **Video capture port:** 40-pin YUV Direct Video Input Port onboard
- **TV output interface:** Supports both RCA jack and S terminal

Panel Link (Optional)

- **Chipset:** Sil 164 PanelLink Digital Transmitter
- **Scalable bandwidth:** Ranging from 25 ~ 112 MHz (VGA ~ SXGA); 24/48-bit one/two pixel per clock

Audio Interface

- **Chipset:** VT82C686A
- **Audio controller:** AC97 ver. 2.0 compliant interface, Multi-stream Direct Sound and Direct Sound 3D acceleration
- **Audio interface:** Microphone in, Line in, CD audio in, line out, Speaker L, Speaker R

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Ethernet Interface

- **Chipset:** Dual Intel 82559ER PCI-bus Ethernet controllers onboard
- **Ethernet interface:** PCI 100/10 Mbps, IEEE 802.3U compatible
- **Remote Boot-ROM:** For diskless system

SSD Interface

One CF socket supports Type I/II Compact Flash Card

Expansion Interface

- **PC/104 connector:** One 16-bit 104-pin connector onboard
- **PCI slot:** One 32-bit PCI slot onboard

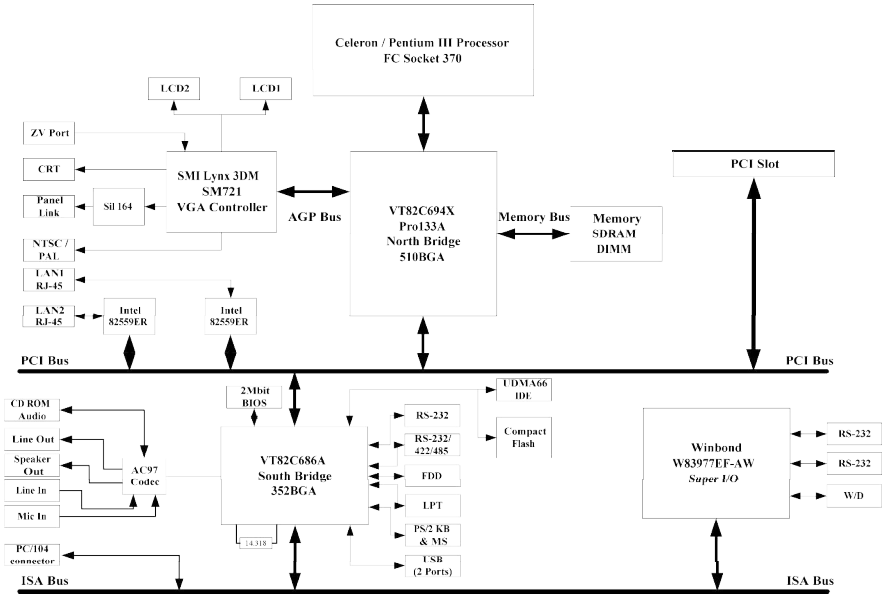
Mechanical and Environmental

- **Power supply voltage:** ATX type, +5V and +12V
- **Typical power requirement:** 5V @ 5.2A, 12V @ 80mA w/ PIII 800MHz & 128MB SDRAM
- **Operating temperature:** 32 to 140°F (0 to 60°C)
- **Board size:** 8"(L) x 5.75"(W) (203mm x 146mm)
- **Weight:** 0.5 Kg

Introduction

1.4 Architecture Overview

The following block diagram shows the architecture and main components of 3307246.



The two key components on board are the VIA VT82C694X North Bridge and VT82C686A super South Bridge. These two devices provide the ISA and PCI bus to which all the major components are attached.

The following sections provide detail information about the functions provided onboard.

1.4.1 VIA VT82C694X

The VIA VT82C694X along with the VT82C686A companion chip provide the basic functionality and buses of the system:

- High Performance CPU interface.
- Full Featured Accelerated Graphics Port (AGP) controller.
- Advanced High-Performance DRAM controller. PC133 compliant SDRAM must be used if 133MHz FSB CPU is to be used.
- Concurrent PCI Bus controller.
- PCI to ISA Bridge provided by VT82C686A super south bridge.
- Universal Serial Bus controller integrated in the VT82C686A.
- UltraDMA-33 / 66 Master Mode PCI EIDE controller. Two connectors are provided: A 40 pin pitch 2.54mm standard IDE interface on the primary controller and a Compact Flash connector on the secondary controller.
- SoundBlaster Pro hardware and Direct Sound ready AC97 Digital Audio controller.

1.4.2 DRAM Interface

The VT82C694X supports eight banks of DRAMs up to 1.5GB. The DRAM controller supports standard Fast Page Mode (FPM) DRAM, EDO-DRAM, Synchronous DRAM (SDRAM) and Virtual Channel SDRAM (VC SDRAM), in a flexible mix / match manner. The Synchronous DRAM interface allows zero wait state bursting between the DRAM and the data buffers at 66/100/133 MHz. The eight banks of DRAM can be composed of an arbitrary mixture of 1M / 2M / 4M / 8M / 16M / 32MxN DRAMs. The DRAM controller also supports optional ECC (single-bit error correction and multi-bit detection) or EC (error checking) capability separately selectable on a bank-by-bank basis. The DRAM controller can run at either the host CPU bus frequency (66 /100 /133MHz) or at the AGP bus frequency (66 MHz) with built-in PLL timing control.

1.4.3 AGP Interface

The VT82C694X system controller also supports full AGP v2.0 capability for maximum bus utilization including 2x and 4x mode transfers, SBA (SideBand Addressing), Flush/Fence commands, and pipelined grants. An eight level request queue plus a four level post-write request queue with thirty-two and sixteen quadwords of read and write data FIFO's respectively are included for deep pipelined and split AGP transactions. A single-level GART TLB with 16 full associative entries and flexible CPU / AGP / PCI remapping control is also provided for operation under protected mode operating environments. Both Windows-95 VXD and Windows-98 / NT5 miniport drivers are supported for interoperability with major AGP-based 3D and DVD-capable multimedia accelerators.

1.4.4 PCI Interface

The VT82C694X supports two 32-bit 3.3 / 5V system buses (one AGP and one PCI) that are synchronous / pseudo-synchronous to the CPU bus. The chip also contains a built-in bus-to-bus bridge to allow simultaneous concurrent operations on each bus. Five levels (doublewords) of post write buffers are included to allow for concurrent CPU and PCI operation. For PCI master operation, forty-eight levels (doublewords) of post write buffers and sixteen levels (doublewords) of prefetch buffers are included for concurrent PCI bus and DRAM/cache accesses. The chip also supports enhanced PCI bus commands such as Memory-Read-Line, Memory-Read-Multiple and Memory-Write-Invalid commands to minimize snoop overhead. In addition, advanced features are supported such as snoop ahead, snoop filtering, L1 write-back forward to PCI master, and L1 write-back merged with PCI post write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

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1.4.5 VIA VT82C686A

The VT82C686A PSIPC (PCI Super-I/O Integrated Peripheral Controller) is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to PCI bus bridge functionality to make a complete Microsoft PC99-compliant PCI/ISA system. In addition to complete ISA extension bus functionality, the VT82C686A includes standard intelligent peripheral controllers:

- Two 16550-compatible serial I/O ports with infrared communications port option on the second port.
- LPT. Support for SPP, EPP and ECP modes.
- Standard floppy disk drive interface.
- Keyboard controller with PS2 mouse support.
- Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.
- Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.
- Full System Management Bus (SMBus) interface.
- Integrated PCI-mastering dual full-duplex direct-sound AC97-link-compatible sound system. Hardware soundblaster-pro and hardware-assisted FM blocks are included for Windows DOS box and real-mode DOS compatibility. Loopback capability is also implemented for directing mixed audio streams into USB and 1394 speakers for high quality digital audio.
- Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.
- Internal I/O APIC (Advanced Programmable Interrupt Controller).

1.4.6 IDE Interface (Bus Master Capability and Synchronous DMA Mode)

Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT82C686A also supports the UltraDMA-33 standard to allow reliable data transfer rates up to 33MB/sec throughput. The VT82C686A also supports the UltraDMA-66 standard. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

Access to these controllers is provided by one standard IDC 40-pin connector and one Compact Flash type II connector.

1.4.7 USB

The Universal Serial Bus controller is USB v1.1 and Universal HCI v1.1 compliant. The VT82C686A includes the root hub with four function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

1.4.8 SMI Lynx3DM SM721 VGA Controller

The Lynx3DM consists of a logic block, which interfaces to a 4MB or 8MB block of integrated memory. The integrated memory supports single clock cycle transfers up to 100MHz. Peak memory bandwidth for the integrated 128-bit memory bus is over 1.6GB/s.

The logic within the Lynx3DM consists of 11 functional blocks: PCI Interface, Host Interface (HIF), Memory Controller, Drawing Engine, Power Down Control Unit, Video Processor, Video Capture Module, LCD Backend Controller, VGA Core, PLL Module, and RAMDAC. A summary of each of the functional blocks, along with important features follows:

- AGP 2X sideband support
- PCI 2.1 compliant
- 33 MHz PCI Master/Slave interface
- Dual aperture feature for concurrent VGA and video/drawing engine access

- Independent memory interface control
- Up to 128-bit memory interface
- Over 1.6GB/s memory bandwidth
- 100MHz single clock/cycle engine
- Designed to accelerate DirectDraw and Direct3D
- IEEE Floating Point Setup Engine
- Complete 3D Rendering Engine set:
  - Bi-linear and tri-linear filtering
  - Mip Mapping
  - Vertex and global fog
  - Source and destination alpha blend
  - Specular highlights
  - Edge anti-aliasing
  - Z-buffering
  - Gouraud shading
  - Mirrored textures
  - Texture decompression
- Offloads motion compensation portion of MPEG-2 decode process from CPU

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- Separate bus master control for motion compensation command and IDCT data
- Sub-picture support
  - 2-bit/pixel format
  - 8-bit/pixel format
- NTSC/PAL interlace mode digital video encoder
- Composite Video and S-Video digital output
- CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- Interlace mode operation
- 2x over-sampling data output to simplify external analog filtering
- Macrovision function (version 7.1.21)
- Closed captioning function
- Dynamic Power Management
- Virtual Refresh
- Standby and Suspend model support
- ACPI, DPMS, APM compliant
- Multiple video windows in HW
- Independent video sources on different displays
- Bi-linear scaling
- Flicker filter and underscan for TV display
- Support for Zoom Video Port interface
- Crop, filter, shrink support
- TFT and DSTN support up to SXGA
- Timing generation for Virtual Refresh
- Popup icon location flexible
- Transparency color support
- 100% IBM VGA compatible
- Separate PLL for LCD panel timing
- 200MHz speed provides resolution support to 1600x1200.

1.4.9 Panel Interface

An alternative display to the standard CRT monitor is digital flat panel interfaces in which the color of each pixel is digitally encoded. The panel data may be transferred in parallel where the color of each pixel is transferred over a number of signal lines at rates up to 80MHz.

Lynx3DM supports both color dual scan STN (passive) and color TFT (active) panel interface. It can also support color TFT panel with RGB analog interface. For color DSTN panel, Lynx3DM can support 16-bit and 24-bit interfaces up to 1600x1200 resolution. For color TFT panel, Lynx3DM can support single pixel per clock of 9-bit, 12-bit, 18-bit, 24-bit, or double-pixel per clock of 24-bit, 36-bit interfaces up to 1280x1024 resolution.

Lynx3DM supports two separate digital LCDs. Both LCDs need to be TFT interface. FP1 has to be only 18-bit TFT interface and FP2 has to be 24-bit TFT interface. DSTN panel can not be supported under dual digital LCD mode. Dual Digital LCD mode is supported through the Virtual Refresh architecture. FP1 and FP2 must be in Virtual Refresh mode. FP1 clocks the data based on VRCLK (Virtual Refresh Clock); whereas FP2 clocks the data based on FIFOCLK (based on Video Clock). The parallel interface is only suitable for short distance (less than 50 cm) and is typically implemented by using of ribbon cables. One should be careful in the EMC design of the box and cabling when this interface is used.

It should also be noted that the signal level of this interface is 3.3V, but does comply with the TTL signal levels. Some - most older displays require 5V signal level.

1.4.10 Zoom Video Port

Lynx3DM's Zoom Video Port (ZV Port) is designed to interface with video solutions implemented as PCMCIA (or PC CardBus) cards: examples are NTSC/PAL decoders, MPEG-2 decoders, and JPEG Codecs. The ZV Port can also directly interface with an NTSC/PAL decoder, such as Philips 7111 or BT819.

Incoming video data from the ZV Port interface can be YUV or RGB format. The data can be interlaced or non-interlaced. The ZV Port can be configured for output if the video capture function is disabled. 18-bit graphics and video data in RGB format can be sent out when the ZV Port is configured for output mode. The ZV Port may also be configured as a test port. Up to 20 signals from each of the logic blocks within Lynx3DM can be brought out to an internal test bus (TD Bus) connected to the ZV Port. System designers or silicon validation engineers can access these signals by setting the TEST0, TEST1, USR0, USR1, and USR2 pins. This approach can bring out a total of 180 internal signals to the primary I/O pins. The test port capability can be used to enhance fault coverage, as well as reduces silicon validation or debugging time.

The Video Capture Unit captures incoming video data from the ZV Port and then stores the data into the frame buffer.

The Video Capture Unit support several features to maintain display quality, and balance the capture rate:

- 2-tap, 3-tap, and 4-tap horizontal filtering
- 2 to 1 and 4 to 1 reduction for horizontal and vertical frame size
- YUV 4:2:2, YUV 4:2:2 with byte swap, RGB 5:5:5, and RGB 5:6:5
- Multiple frame skipping methods
- Interlaced data and non-interlaced data capture
- Single buffer and double buffer capture
- Cropping

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Lynx3DM uses the Video Processor block to display the captured data on the LCD, TV, or CRT display. The captured data can be displayed through Video Window I or Video Window II. The stretching, color interpolation, YUV-to-RGB conversion, and color key functions are performed in the Video Processor. Lynx3DM's Video Processor can simultaneously process captured video data and perform CD-ROM playback on two independent video windows.

Lynx3DM also supports real-time video capture to the hard drive or system memory through PCI master mode or slave mode. In PCI bus master mode, Lynx3DM uses the Drawing Engine's Host BLT and Host DMA functions to maximize performance.

1.4.11 TV Encoder

The TV Encoder is an NTSC/PAL Composite Video/S-video Encoder. It receives RGB inputs and converts to digital video signals based on CCIR 624 format.

The input video signal of the TV Encoder is RGB 8-bit each. The sampling rate is corresponding to CCIR 601, Square pixel and 4Fsc (NTSC only).

The output video signals of the TV Encoder are Composite video signal and S-video signals of 10-bit each. These output signals are over-sampled by a double frequency clock called CLKX2. This feature helps to simplify external analog filtering.

The TV Encoder video timing is controlled by vertical sync and the horizontal sync input signals. The blank signal input is optional. If the blank signal input signal is pulled up, internal blanking control will be performed.

Macrovision 7.01 and closed captioning functions are included.

Key features are summarized as the following:

- „ NTSC/PAL interlace mode digital video encoder
- „ Composite Video and S-Video digital output
- „ CCIR 601, Square pixel and 4Fsc (NTSC only) resolution RGB input
- „ Slave timing operation
- „ Interlace mode operation
- „ 2x over-sampling data output to simplify external analog filtering
- „ Selectable pedestal level OIRE/7.5IRE for NTSC
- „ Macrovision function (version 7.01)
- „ Closed aptioning unction

1.4.12 Ethernet

The Ethernet interfaces are based on two Intel 82559ER Ethernet controllers, which support both 100Mbit as well as l0Mbit Base-T interface.

The Ethernet controllers are attached to the PCI bus and use PCI bus mastering for data transfer. The CPU is thereby not loaded during the actual data transfer.

The 82559ER is part of Intel's second generation family of fully integrated 10BASE-T / 100BASE-TX LAN solutions. The 82559ER consists of both the Media Access Controller (MAC) and the physical layer (PHY) combined into a single component solution. 82559 family members build on the basic functionality of the 82558 and contain power management enhancements.

The 82559ER is a 32-bit PCI controller that features enhanced scatter-gather bus mastering capabilities, which enables the 82559ER to perform high-speed data transfers over the PCI bus. The 82559ER bus master capabilities enable the component to process high-level commands and perform multiple operations, thereby off-loading communication tasks from the system CPU. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns, allowing the 82559ER to transmit data with minimum interframe spacing (IFS).

The 82559ER can operate in either full duplex or half duplex mode. In full duplex mode the 82559ER adheres to the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.

The 82559ER includes a simple PHY interface to the wire transformer at rates of 10BASE-T and 100BASE-TX, and Auto-Negotiation capability for speed, duplex, and flow control. These features and others reduce cost, real estate, and design complexity.

The 82559ER also includes an interface to a serial (4-pin) EEPROM and a parallel interface to a 128 Kbyte Flash memory. The EEPROM provides power-on initialization for hardware and software configuration parameters

1.4.13 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

1.4.14 Panel Link Interface (Optional)

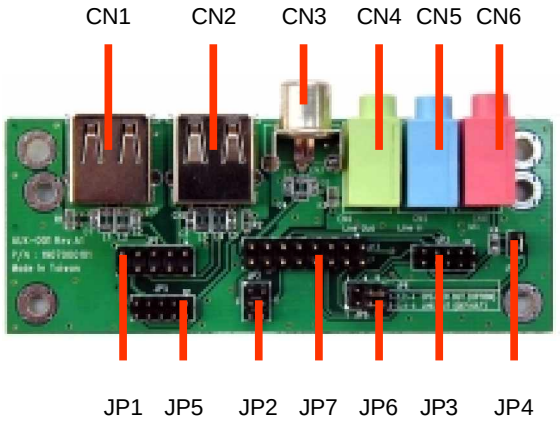
The SiI164 transmitter uses PanelLink® Digital technology to support displays ranging from VGA to UXGA resolutions (25 - 165Mpps) in a single link interface. The SiI164 transmitter has a highly flexible interface with either a 12-bit mode (½ pixel per clock edge) or 24-bit mode 1-pixel/clock input for true color (16.7 million) support. In 24-bit mode, the SiI164 supports single or dual edge clocking. In 12-bit mode, the SiI164 supports dual edge single clocking or single edge dual clocking. The SiI164 can be programmed though an I2C interface. The SiI164 support Receiver and Hot Plug Detection.

PanelLink Digital technology simplifies PC design by resolving many of the system level issues associated with high-speed mixed signal design, providing the system designer with a digital interface solution that is quicker to market and lower in cost.

2. Hardware Configuration Setting

This chapter explains you the instructions of how to setup your system.

2.1 Audio / USB Daughter Board Jumper & Connector Layout



2.2 Audio / USB Daughter Board Jumper & Connector List

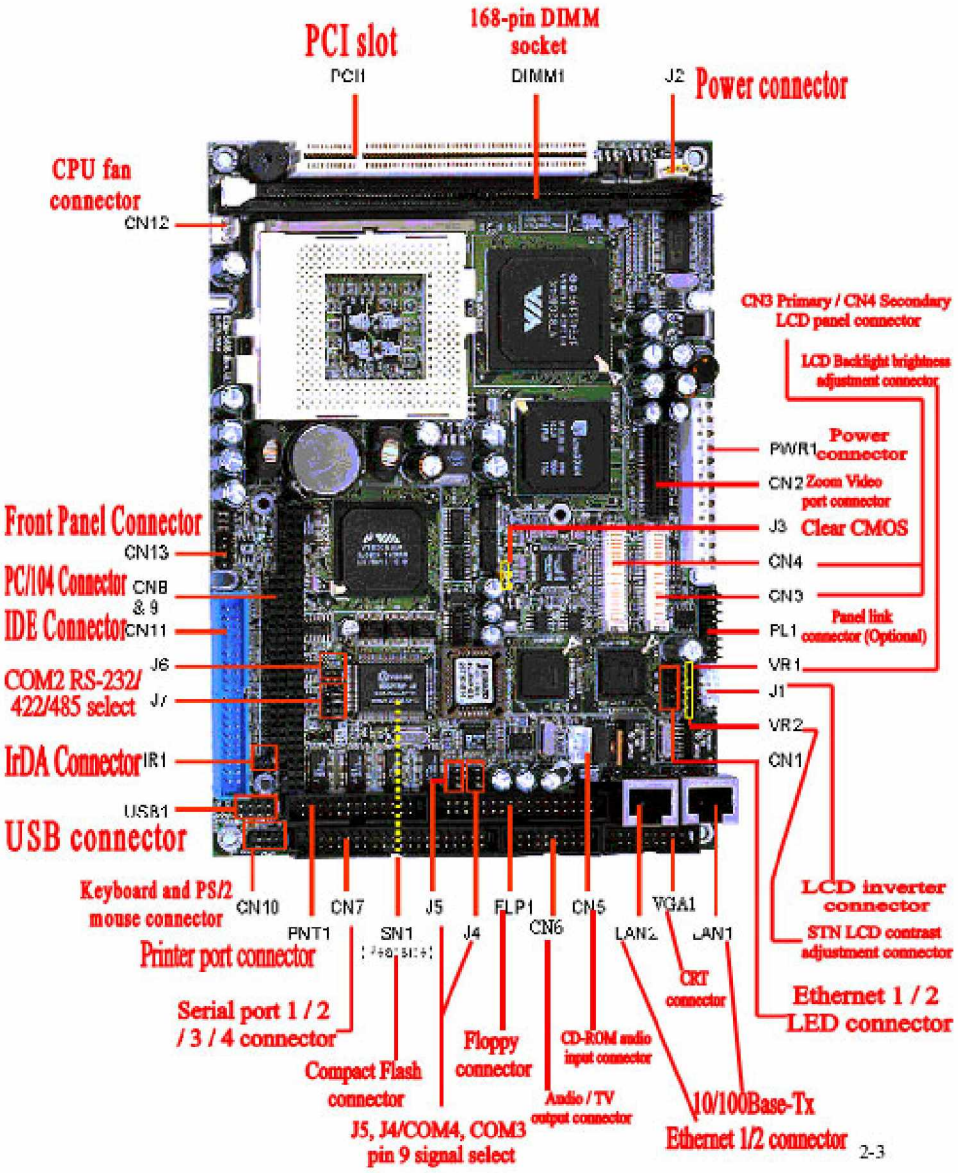
Jumpers		
Label	**Function**	**Note**
JP1	2.54mm pitch USB connector for Mini module series	5 x 2 header, pitch 2.54mm
JP2	Reserve for S-terminal testing	3 x 2 header, pitch 2.0mm
JP3	Audio connector for Micro module series	5 x 2 header, pitch 2.0mm
JP4	Reserved	
JP5	2.00mm pitch USB connector for Micro module series	5 x 2 header, pitch 2.0mm
JP6	Line out / Speaker out select	1-3, 2-4 Speaker out 3-5, 4-6 Line out (Default)
JP7	TV / Audio connector for Mini module series	8 x 2 header, pitch 2.54mm

Hardware Configuration Setting

Connectors		
Label	**Function**	**Note**
CN1	USB 1 connector	
CN2	USB 2 connector	
CN3	TV output RCA jack	
CN4	Line out or Speaker out	Select by JP6
CN5	Line in	
CN6	Mic in	

Hardware Configuration Setting

2.3 Main Board Jumpers & Connectors Layout Diagram



Hardware Configuration Setting

2.4 Main Board Jumpers & Connectors List

Connectors on the board are linked to external devices such as hard disk drives, keyboard, mouse, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

The following tables list the function of each of the board's jumpers and connectors.

Jumpers		
Label	**Function**	**Note**
J1	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
J2	Power connector	3 x 1 wafer, pitch 2.54mm
J3	Clear CMOS	3 x 1 header, pitch 2.54mm
J4	COM4 pin 9 signal select	3 x 2 header, pitch 2.0mm
J5	COM3 pin 9 signal select	3 x 2 header, pitch 2.0mm
J6, J7	COM2 RS-232/422/485 select	3 x 2 header, pitch 2.0mm 4 x 3 header, pitch 2.0mm (J7)
J8	Reserve for future use	3 x 3 header, pitch 2.0mm

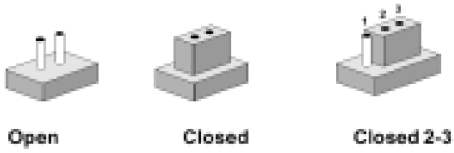
Connectors		
Label	**Function**	**Note**
CN1	Ethernet 1 / 2 LED connector	5 x 2 header, pitch 2.54mm
CN2	Zoom Video port connector	Samtec CLM-120-02-L-D
CN3	Primary LCD panel connector	HIROSE DF13-40DP-1.25V
CN4	Secondary LCD panel connector	HIROSE DF13-40DP-1.25V
CN5	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
CN6	Audio / TV output connector	8 x 2 header, pitch 2.54mm
CN7	Serial port 1 / 2 / 3 / 4 connector	20 x 2 header, pitch 2.54mm
CN8, 9	PC/104 connector	
CN10	Keyboard and PS/2 mouse connector	4 x 2 header, pitch 2.54mm
CN11	IDE device connector	20 x 2 header, pitch 2.54mm
CN12	CPU fan connector	3 x 1 wafer, pitch 2.54mm
CN13	Front panel connector	4 x 2 header, pitch 2.54mm
FLP1	Floppy connector	17 x 2 header, pitch 2.54mm
IR1	IrDA connector	3 x 2 header, pitch 2.0mm
LAN1	10/100Base-Tx Ethernet 1 connector	RJ-45
LAN2	10/100Base-Tx Ethernet 2 connector	RJ-45 (3307246 only)
PL1	Panel link connector (Optional)	8 x 2 header, pitch 2.54mm
PNT1	Printer port connector	13 x 2 header, pitch 2.54mm
PWR1	Power connector	
SN1	Compact Flash connector	
USB1	USB connector	5 x 2 header, pitch 2.0mm
VGA1	CRT connector	8 x 2 header, pitch 2.54mm
VR1	LCD Backlight brightness adjustment connector	3 x 1 header, pitch 2.54mm
VR2	STN LCD contrast adjustment connector	3 x 1 header, pitch 2.54mm
DIM1	168-pin DIMM socket	

Hardware Configuration Setting

2.5 Setting Jumpers

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

A pair of needle-nose pliers may be helpful when working with jumpers.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

2.5.1 Clear CMOS (J3)

You can use J3 to clear the CMOS data if necessary. To reset the CMOS data, set J3 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed.

Clear CMOS (J3)		
	Protect*	Clear CMOS
J3	1 2 3 	1 2 3 

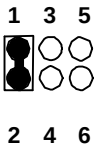
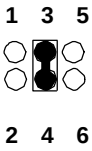
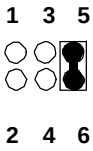
* default

Hardware Configuration Setting

2.5.2 COM3 / 4 Pin 9 Signal Select (J5 / J4)

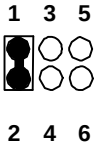
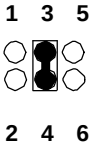
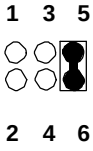
The 3307246 COM3 / 4 pin 9 signal can be selected as +12V, +5V, or Ring by setting J5 / J4.

COM3 Pin 9 Signal Select (J5)

	+12V	+5V	Ring*
J5			

* default

COM4 Pin 9 Signal Select (J4)

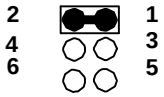
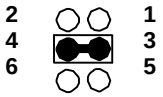
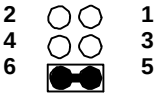
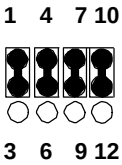
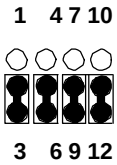
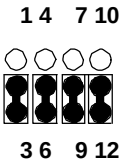
	+12V	+5V	Ring*
J4			

* default

2.5.3 COM2 RS-232/422/485 Select (J6, J7)

The 3307246 COM2 serial port can be selected as RS-232, RS-422, or RS-485 by setting J6 & J7.

COM2 RS/232/422/485 Select (J6, J7)

	RS-232*	RS-422	RS-485
J6			
J7			

* default

2.6 Connector Definitions

2.6.1 Power Connector 1 (PWR1)

Signal	PIN
NC	1
VCC	2
+12V	3
-12V	4
GND	5
GND	6
GND	7
GND	8
-5V	9
VCC	10
VCC	11
VCC	12

2.6.2 LCD Inverter Connector (J1)

Signal	PIN
VCC	5
VR	4
ENBKL	3
GND	2
+12V	1

Note: For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal (pin 4) controlled by **VR1**. Please see the VR1 section for detailed circuitry information.

2.6.3 Signal Configuration – LCD Inverter Connector (J1)

VR	Vadj = 5V ~ 0V.
ENBKL	LCD backlight ON/OFF control signal.

2.6.4 Auxiliary Power Connector (J2)

Signal	PIN
VCCSB	3
VCC	2
PSON#	1

Note:

Set J2 to 2-3 closed. If AT power supply is to be used.

2.6.5 Ethernet 1 / 2 LED Connector (CN1)

Signal	PIN		Signal
NC	10	9	NC
SPDLED2#	8	7	VCC3SB
LILED2#	6	5	ACTLED2#
SPDLED1#	4	3	VCC3SB
LILED1#	2	1	ACTLED1#

2.6.6 Signal Description – Ethernet 1 / 2 LED Connector (CN1)

ACTLED1# / 2#	Activity LED. The Activity LED pin indicates either transition or reception activity. When activity is present, the activity LED is on; when no activity is present, the activity LED is off.
LILED1# / 2#	Link Integrity LED. The Link Integrity LED pin indicates link integrity. If the link is valid in either 10 or 100 Mbps, the LED is on; if link is invalid, the LED is off.
SPDLED1# / 2#	Speed LED. The Speed LED pin indicates the speed. The speed LED will be on at 100 Mbps and off at 10 Mbps.

2.6.7 Zoom Video Port Connector (CN2)

Signal	PIN		Signal
GND	1	2	P0
GND	3	4	P1
GND	5	6	P2
GND	7	8	P3
GND	9	10	P4
GND	11	12	P5
GND	13	14	P6
GND	15	16	P7
GND	17	18	P8
GND	19	20	P9
NC	21	22	P10
NC	23	24	P11
NC	25	26	P12
NC	27	28	P13
NC	29	30	P14
NC	31	32	P15
DDCCLK	33	34	BLANK
DDCDAT	35	36	HREF
3.3V	37	38	PCLK
3.3V	39	40	VREF

2.6.8 Signal Description – Zoom Video Port Connector (CN2)

P [0:15]	RGB or YUV input / RGB digital output
PCLK	Pixel clock
VREF	Vsync input from PC Card or video decoder
HREF	Hsync input from PC Card or video decoder
BLANK	Blank output. 0 = BLANK output
DDCCLK	USR1/ DDC2/ I²C Clock for CRT
DDCDAT	USR0/ DDC2/ I²C Data for CRT

2.6.9 Video Port Interface I/O Compliance

24-bit TFT	ZV Port (Input mode)	I/O	NSTL/PAL Decoder (Input mode)	I/O	Graphics/Video (Output mode)	I/O
	VS	I	VS	I	R7	O
HREF	HREF	I	HREF	I	R6	O
BLANK	(Note 1)		(Note 1)		BLANK	O
PCLK	PCLK	I	PCLK	I	PCLK	O
P15	Y7	I	R7	I	R5	O
P14	Y6	I	R6	I	R4	O
P13	Y5	I	R5	I	R3	O
P12	Y4	I	R4	I	R2	O
P11	Y3	I	R3	I	G7	O
P10	Y2	I	G7	I	G6	O
P9	Y1	I	G6	I	G5	O
P8	Y0	I	G5	I	G4	O
P7	UV7	I	G4	I	G3/Vindex_[7]	O
P6	UV6	I	G3	I	G2/Vindex_[6]	O
P5	UV5	I	G2	I	G7/Vindex_[5]	O
P4	UV4	I	B7	I	G6/Vindex_[4]	O
P3	UV3	I	B6	I	G5/Vindex_[3]	O
P2	UV2	I	B5	I	G4/Vindex_[2]	O
P1	UV1	I	B4	I	G3/Vindex_[1]	O
P0	UV0	I	B3	I	G2/Vindex_[0]	O

Note 1: BLANK pin can used as TVCLK output, which is independent of ZV port.

Note 2: Vindex [7:0] is indexed video port.

Note 3: SMI test bus is for internal use only.

2.6.10 Primary LCD Panel Connector (CN3)

Signal	PIN		Signal
VDDSAFE5	2	1	VDDSAFE5
GND	4	3	GND
VDDSAFE3	6	5	VDDSAFE3
GND	8	7	Vcon
P1	10	9	P0
P3	12	11	P2
P5	14	13	P4
P7	16	15	P6
P9	18	17	P8
P11	20	19	P10
P13	22	21	P12
P15	24	23	P14
P17	26	25	P16
P19	28	27	P18
P21	30	29	P20
P23	32	31	P22
GND	34	33	GND
FLM	36	35	SHFCLK
LP	38	37	M
ENVEE	40	39	ENBKL

2.6.11 Secondary LCD Panel Connector (CN4)

Signal	PIN		Signal
VDDSAFE5	2	1	VDDSAFE5
GND	4	3	GND
VDDSAFE3	6	5	VDDSAFE3
GND	8	7	Vcon
P25	10	9	P24
P27	12	11	P26
P29	14	13	P28
P31	16	15	P30
P33	18	17	P32
P35	20	19	P34
P37	22	21	P36
P39	24	23	P38
P41	26	25	P40
P43	28	27	P42
P45	30	29	P44
P47	32	31	P46
GND	34	33	GND
P23	36	35	LVDSCLK
P22	38	37	P15
ENVEE	40	39	ENBKL

2.6.12 Signal Description – Primary & Secondary LCD Panel Connector (CN3, CN4)

P [47:0]	Flat Panel Data Bit 47 to Bit 0 for single panel implementation. For Dual Panel Implementation Panel 1: P21-16, P13-8, P5-0, panel1data Panel 2: P23, LP2 / HSYNC2 P22, FLM2 / VSYNC2 P15, M2 P47-P24, panel 2 data Note: P14, P7, P6 are not used for Dual Panel Implementation. LVDSCLK used as SHFCLK2. Flat panel data output for 9, 12, 18, 24, 12 x 2, or 18 x 2 bit TFT flat panels. Refer to table below for configurations for various panel types. The flat panel data and control outputs are all on-board controlled for secure power-on/off sequencing
SHFCLK	Shift Clock. Pixel clock for flat panel data
LVDSCLK	This pin is used as SHFCLK2 for dual panel configuration
LP	Latch Pulse. Flat panel equivalent of HSYNC (horizontal synchronization)
FLM	First Line Marker. Flat panel equivalent of VSYNC (vertical synchronization)
M	Multipurpose signal, function depends on panel type. May be used as AC drive control signal or as BLANK# or Display Enable signal
ENBKL	Enable backlight signal. This signal is controlled as a part of the panel power sequencing
ENVEE	Enable VEE. Signal to control the panel power-on/off sequencing. A high level may turn on the VEE (LCD bias voltage) supply to the panel

2.6.13 Signal Configuration – DSTN & TFT Panel Displays

	DSTN				TFT			
Pin name	16-bit	24-bit	9-bit	12-bit	18-bit	24-bit	12-bit x 2	18-bit x 2
P35								RB5
P34								RB4
P33								RA5
P32								RA4
P31								GB5
P30								GB4
P29								GA5
P28								GA4
P27								BB5
P26								BB4
P25								BA5
P24								BA4
P23		UD11				R7	RB3	RB3
P22		UD10				R6	RB2	RB2
P21		UD9			R5	R5	RB1	RB1
P20		UD8			R4	R4	RB0	RB0
P19	UD7	UD7		R3	R3	R3	RA3	RA3
P18	UD6	UD6	R2	R2	R2	R2	RA2	RA2
P17	UD5	UD5	R1	R1	R1	R1	RA1	RA1
P16	UD4	UD4	R0	R0	R0	R0	RA0	RA0
P15	UD3	UD3				G7	GB3	GB3
P14	UD2	UD2				G6	GB2	GB2
P13	UD1	UD1			G5	G5	GB1	GB1
P12	UD0	UD0			G4	G4	GB0	GB0
P11		LD11		G3	G3	G3	GA3	GA3
P10		LD10	G2	G2	G2	G2	GA2	GA2
P9		LD9	G1	G1	G1	G1	GA1	GA1
P8		LD8	G0	G0	G0	G0	GA0	GA0
P7	LD7	LD7				B7	BB3	BB3
P6	LD6	LD6				B6	BB2	BB2
P5	LD5	LD5			B5	B5	BB1	BB1
P4	LD4	LD4			B4	B4	BB0	BB0
P3	LD3	LD3		B3	B3	B3	BA3	BA3
P2	LD2	LD2	B2	B2	B2	B2	BA2	BA2
P1	LD1	LD1	B1	B1	B1	B1	BA1	BA1
P0	LD0	LD0	B0	B0	B0	B0	BA0	BA0

Pin name	24-bit x 2 TFT	TFTs: FP1 + FP2	18-bit x 2 TFT	24-bit TFT
P47	RB7	FP2_R7		
P46	RB6	FP2_R6		
P45	RA7	FP2_R5		
P44	RA6	FP2_R4		
P43	GB7	FP2_R3		
P42	GB6	FP2_R2		
P41	GA7	FP2_R1		
P40	GA6	FP2_R0		
P39	BB7	FP2_G7		
P38	BB6	FP2_G6		
P37	BA7	FP2_G5		
P36	BA6	FP2_G4		
P35	RB5	FP2_G3	RB5	
P34	RB4	FP2_G2	RB4	
P33	RA5	FP2_G1	RA5	
P32	RA4	FP2_G0	RA4	
P31	GB5	FP2_B7	GB5	
P30	GB4	FP2_B6	GB4	
P29	GA5	FP2_B5	GA5	
P28	GA4	FP2_B4	GA4	
P27	BB5	FP2_B3	BB5	
P26	BB4	FP2_B2	BB4	
P25	BA5	FP2_B1	BA5	
P24	BA4	FP2_B0	BA4	
P23	RB3	FP2_VSYNC	RB3	R7
P22	RB2	FP2_HSYNC	RB2	R6
P21	RB1	FP1_R5	RB1	R5
P20	RB0	FP1_R4	RB0	R4
P19	RA3	FP1_R3	RA3	R3
P18	RA2	FP1_R2	RA2	R2
P17	RA1	FP1_R1	RA1	R1
P16	RA0	FP1_R0	RA0	R0
P15	GB3	FP2_DE	GB3	G7
P14	GB2		GB2	G6
P13	GB1	FP1_G5	GB1	G5
P12	GB0	FP1_G4	GB0	G4
P11	GA3	FP1_G3	GA3	G3
P10	GA2	FP1_G2	GA2	G2

Pin name	24-bit x 2 TFT	TFTs: FP1 + FP2	18-bit x 2 TFT	24-bit TFT
P9	GA1	FP1_G1	GA1	G1
P8	GA0	FP1_G0	GA0	G0
P7	BB3		BB3	B7
P6	BB2		BB2	B6
P5	BB1	FP1_B5	BB1	B5
P4	BB0	FP1_B4	BB0	B4
P3	BA3	FP1_B3	BA3	B3
P2	BA2	FP1_B2	BA2	B2
P1	BA1	FP1_B1	BA1	B1
P0	BA0	FP1_B0	BA0	B0

Note:

The principle of attachment of TFT panels is that the bits for red, green, and blue use the least significant bits and skip the most significant bits if the display interface width of the TFT panel is insufficient.

2.6.14 CD-ROM Audio Input Connector (CN5)

Signal	PIN
CD_R	4
CD_GND	3
CD_L	2
CD_GND	1

2.6.15 Signal Configuration – CD-ROM Input Connector (CN5)

CD L/R	Left and right CD audio input lines.
CD_GND	GND for left and right CD. This GND level is not connected to the board GND.

2.6.16 Audio / TV Output Connector (CN6)

Signal	PIN		Signal
COMP	16	15	GND
Cout	14	13	GND
Yout	12	11	AGND
Line-In R	10	9	Line-In L
SPK R	8	7	SPK L
Line-Out R	6	5	Line-Out L
AGND	4	3	AGND
Mic Bias	2	1	Mic

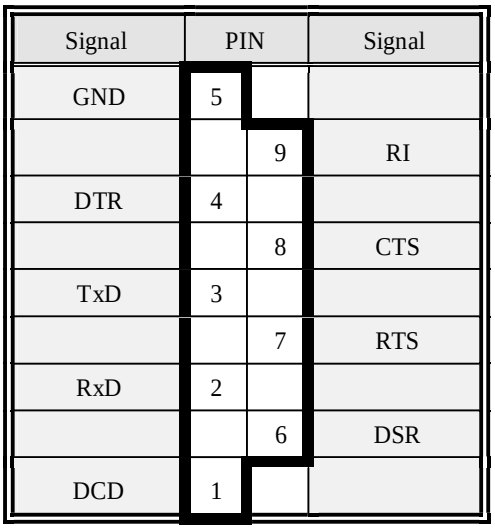
2.6.17 Signal Description – Audio / TV Output Connector (CN6)

SPK L/R	Left and right speaker output. These are the speaker outputs directly from the speaker amplifier. Coupling capacitors must be used in order to avoid DC-currents in the speakers. If the Audio Bracket is used these signals are supplied on the PCB. GND should be used as return for each speaker. Maximum power: 0.5W@4 Ω load for each channel.
Mic / Mic Bias	The MIC signal is used for microphone input. This input is fed to the left microphone channel. Mic Bias provides 3.3V supplied through 3.2K Ω with capacitive decoupling to GND. This signal may be used for bias of some microphone types.
Line-In L/R	Left and right line in signals.
Line-Out L/R	Left and right line out signals. Both signals are capacitor coupled and should have GND as return.
Yout	Luminance output
Cout	Chrominance output
COMP	Composite video output

2.6.18 Pin Header Serial Port 1 / 2 / 3 / 4 Connector in RS-232 Mode (CN7)

Signal	PIN		Signal
NC	40	39	RI4/5V /12V
CTS4	38	37	RTS4
DSR4	36	35	GND
DTR4	34	33	TxD4
RxD4	32	31	DCD4
NC	30	29	RI3/5V /12V
CTS3	28	27	RTS3
DSR3	26	25	GND
DTR3	24	23	TxD3
RxD3	22	21	DCD3
NC	20	19	RI2
CTS2	18	17	RTS2
DSR2	16	15	GND
DTR2	14	13	TxD2
RxD2	12	11	DCD2
NC	10	9	RI1
CTS1	8	7	RTS1
DSR1	6	5	GND
DTR1	4	3	TxD1
RxD1	2	1	DCD1

2.6.19 Serial Port 1 / 2 / 3 / 4 with External DB9 Connector



Signal	PIN		Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

2.6.20 Signal Description – Serial Port 1 / 2 / 3 / 4 Connector in RS-232 Mode (CN7)

TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone-ringing signal.

2.6.21 Pin Header Serial Port 2 Connector (CN7 / Pin 11~20) in RS422 Mode

Signal	PIN		Signal
NC	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
TxD+	4	3	TxD-
RxD-	2	1	RxD+

2.6.22 Signal Description – Serial Port 2 in RS422 Mode

TxD +/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the TxD line driver is enabled through the Serial Port 2's DTR signal. (Modem control register)
RxD +/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.
RTS +/-	Request To Send. The level of this differential signal pair output is controlled through the Serial Port 2's RTS signal (Modem control register). The RTS line driver is enabled through the Serial Port 2's CSE signal.
CTS +/-	Clear To Send. The level of this differential signal pair input could be read from the Serial Port 2's CTS signal. (Modem control register)

2.6.23 Pin Header Serial Port 2 Connector (CN7 / Pin 11~20) in RS485 Mode

Signal	PIN		Signal
NC	10	9	CTS/RTS +
NC	8	7	CTS/RTS -
NC	6	5	GND
RxD/TxD +	4	3	RxD/TxD -
NC	2	1	NC

2.6.24 Signal Description – Serial Port 2 in RS485 Mode

RxD/TxD +/-	Bi-directional data signal pair. Received data is available in Serial Port 2 Receiver Buffer Register. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication line, if the TxD line driver is enabled through the Serial Port 2's DTR signal (Modem control register). The data transmitted will simultaneously be received the in Serial Port 2 Receiver Buffer Register.
CTS/RTS +/-	Bi-directional control signal pair. The level of this differential signal pair could be read from the Serial Port 1's CTS signal (Modem control register). The level of this differential signal pair could be controlled through the Serial Port 2's RTS signal (Modem control register). The control signal line driver is enabled through the Serial Port 2's CSE signal.

Warning: Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperature reaches 150 °C.

RS422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typ. 100-120 **Ω**). The resistors could be placed in the connector housing.

RS485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 **Ω**). Stubs to substations should be avoided.

Hardware Configuration Setting

2.6.25 PC104 Connector (CN8, CN9)

Signal	PIN		PIN		Signal
GND	B32	A32			GND
GND	B31	A31			SA0
OSC	B30	A30			SA1
VCC	B29	A29			SA2
BALE	B28	A28			SA3
NC			C19	D19	GND
TC	B27	A27			SA4
SD15			C18	D18	GND
DACK2#	B26	A26			SA5
SD14			C17	D17	MASTER#
IRQ3	B25	A25			SA6
SD13			C16	D16	VCC
IRQ4	B24	A24			SA7
SD12			C15	D15	DRQ7
IRQ5	B23	A23			SA8
SD11			C14	D14	DACK7#
IRQ6	B22	A22			SA9
SD10			C13	D13	DRQ6
IRQ7	B21	A21			SA10
SD9			C12	D12	DACK6#
SYSCLK	B20	A20			SA11
SD8			C11	D11	DRQ5
REFRESH#	B19	A19			SA12
SMEMW#			C10	D10	DACK5#
DRQ1	B18	A18			SA13
SMEMR#			C9	D9	DRQ0
DACK1#	B17	A17			SA14
LA17			C8	D8	DACK0#
DRQ3	B16	A16			SA15
LA18			C7	D7	IRQ14
DACK3#	B15	A15			SA16
LA19			C6	D6	IRQ15
IOR#	B14	A14			SA17
LA20			C5	D5	IRQ12
IOW#	B13	A13			SA18
LA21			C4	D4	IRQ11
SMEMR#	B12	A12			SA19
LA22			C3	D3	IRQ10
SMEMW#	B11	A11			AEN
LA23			C2	D2	IOCS16#
GND	B10	A10			IOCHRDY
SBHE#			C1	D1	MEMCS16#
+ 12 V	B9	A9			SD0
GND			C0	D0	GND
OWS#	B8	A8			SD1
- 12 V	B7	A7			SD2
DRQ2	B6	A6			SD3
- 5 V	B5	A5			SD4
IRQ9	B4	A4			SD5
VCC	B3	A3			SD6
RESETDRV	B2	A2			SD7
GND	B1	A1			IOCHCHK#

2.6.26 Signal Description – PC104 Connector (CN8, CN9)

2.6.26.1 Address

LA [23:17]	The address signals LA [23:17] define the selection of a 128KB section of memory space within the 16MB address range of the 16-bit data bus. These signals are active high. The validity of the MEMCS16# depends on these signals only. These address lines are presented to the system with tri-state drivers. The permanent master drives these lines except when an alternate master cycle occurs; in this case, the temporary master drives these lines. The LA signals are not defined for I/O accesses.
SA [19:0]	System address. Address lines for the first one Megabyte of memory. SA [9:0] used for I/O addresses. SA0 is the least significant bit
SBHE#	This signal is an active low signal, which indicates that a byte is being transferred on the upper byte (SD [15:8]) of the 16-bit bus. All bus masters will drive this line with a tri-state driver.

2.6.26.2 Data

SD [15:8]	These signals are defined for the high order byte of the 16-bit data bus. Memory or I/O transfers on this part of the bus are defined when SBHE# is active.
SD [7:0]	These signals are defined for the low order byte of the 16-bit data bus being the only bus for 8 bit PC-AT/PC104 adapter boards. Memory or I/O transfers on this part of the data bus are defined for 8-bit operations with even or odd addresses and for 16-bit operations for odd addresses only. The signals SA0 and SBHE# are used to define the data present on this bus:

SBHE#	SA0	SD15-SD8	SD7-SD0	Action
0	0	ODD	EVEN	Word transfer
0	1	ODD	ODD	Byte transfer on SD15-SD8
1	0	-	EVEN	Byte transfer on SD7-SD0
1	1	-	ODD	Byte transfer on SD7-SD0

2.6.26.3 Commands

BALE	This is an active high signal used to latch valid addresses from the current bus master on the falling edge of BALE. During DMA, refresh and alternate master cycles, BALE is forced high for the duration of the transfer. The permanent master drives BALE with a totem-pole driver.
IOR#	This is an active low signal driven by the current master to indicate an I/O read operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
IOW#	This is an active low signal driven by the current master to indicate an I/O writes operation. I/O mapped devices using this strobe for selection should decode addresses SA [15:0] and AEN. Additionally, DMA devices will use IOR# in conjunction with $DACK_n$# to decode a DMA transfer from the I/O device. The current bus master will drive this line with a tri-state driver.
SMEMR#	This is an active low signal driven by the permanent master to indicate a memory read operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
SMEMW#	This is an active low signal driven by the permanent master to indicate a memory write operation in the first 1MB of system memory. Memory mapped devices using this strobe should decode addresses SA [19:0] only. If an alternate master drives MEMR#, the permanent master will drive SMEMR# delayed by internal logic. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMR#	This is an active low signal driven by the current master to indicate a memory read operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.
MEMW#	This is an active low signal driven by the current master to indicate a memory write operation. Memory mapped devices using this strobe should decode addresses LA [23:17] and SA [19:0]. All bus masters will drive this line with a tri-state driver. The permanent master ties this line to VCC through a pull-up resistor to ensure that it is inactive during the exchange of bus masters.

2.6.26.4 Transfer Response

IOCS16#	This is an active low signal driven by an I/O-mapped PC-AT/PC104 adapter indicating that the I/O device located at the address is a 16-bit device. This open collector signal is driven, based on SA [15:0] only (not IOR# and IOW#) when AEN is not asserted.
MEMCS16#	This is an active low signal driven by a memory mapped PC-AT/PC104 adapter indicating that the memory device located at the address is a 16-bit device. This open collector signal is driven, based on LA [23:17] only.
0WS#	This signal is an active low open-collector signal asserted by a 16-bit memory mapped device that may cause an early termination of the current transfer. It should be gated with MEMR# or MEMW# and is not valid during DMA transfers. IOCHRDY precedes 0WS#.
IOCHRDY	This is an active high signal driven inactive by the target of either a memory or an I/O operation to extend the current cycle. This open collector signal is driven based on the system address and the appropriate control strobe. IOCHRDY precedes 0WS#.
IOCHCK#	This is an active low signal driven active by a PC-AT/PC104 adapter detecting a fatal error during bus operation. When this open collector signal is driven low it will typically cause a non-mask able interrupt.

2.6.26.5 Controls

SYSCLK	This clock signal may vary in frequency from 2.5 MHz to 25.0 MHz depending on the set-up made in the BIOS. Frequencies above 16 MHz are not recommended. The standard states 6 MHz to 8.33 MHz, but most new adapters are able to handle higher frequencies. The PC-AT/PC104 bus timing is based on this clock signal.
OSC	This is a clock signal with a 14.31818 MHz ± 50 ppm frequency and a 50 ± 5% duty cycle. The permanent master drives the signal.
RESETDRV	This active high signal indicates that the adapter should be brought to an initial reset condition. This signal will be asserted by the permanent master on the bus for at least 100 ms at power-up or watchdog time-out to ensure that adapters in the system are properly reset. When active, all adapters should turn off or tri-state all drivers connected to the bus.

2.6.26.6 Interrupts

IRQ [3:7], IRQ [9:12], IRQ [14:15]	These signals are active high signals, which indicate the presence of an interrupting PC-AT/PC104 bus adapter. Due to the use of pull-ups, unused interrupt inputs must be masked.

2.6.26.7 Bus Arbitration

DRQ [0:3], DRQ [5:7]	These signals are active high signals driven by a DMA bus adapter to indicate a request for a DMA bus operation. DRQ [0:3] request 8 bit DMA operations, while DRQ [5:7] request 16 bit operations. All bus DMA adapters will drive these lines with a tri-state driver. The permanent master monitors these signals to determine which of the DMA devices, if any, are requesting the bus.
DACK [0:3]#, DACK [5:7]#	These signals are active low signals driven by the permanent master to indicate that a DMA operation can begin. A totem pole driver for DMA channels attached continuously drives them.
AEN	This signal is an active high totem pole signal driven by the permanent master to indicate that the DMA controller drives the address lines. The assertion of AEN disables response to I/O port addresses when I/O command strobes are asserted. AEN being asserted, only the device with active $DACK_n$# should respond.
REFRESH#	This is an active low signal driven by the current master to indicate a memory refresh operation. The current master will drive this line with a tri-state driver.
TC	This active high signal is asserted during a read or writes command indicating that the DMA controller has reached a terminal count for the current transfer. $DACK_n$# must be presented by the bus adapter to validate the TC signal.
MASTER#	This signal is not supported by the chipset.

2.6.27 Keyboard and PS/2 Mouse Connector (CN10)

Signal	PIN		Signal
		4	NC
MCLK	7	3	MDAT
VCC	6	2	GND
KCLK	5	1	KDAT

2.6.28 Signal Description – Keyboard / Mouse Connector (CN10)

KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.
MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

2.6.29 IDE Device Connector (CN11)

Signal	PIN		Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDDRQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PDRDY	27	28	GND
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	NC
PDA0	35	36	PDA2
PDCS1#	37	38	PDCS3#
PDDACT#	39	40	GND

2.6.30 Signal Description – IDE Device Connector (CN11)

PDA [2:0]	Primary Disk Address. PDA [2:0] are used to indicate which byte in either the ATA command block or control block is being accessed.
PDCS1#	Primary Master Chip Select. This signal corresponds to CS1FX# on the primary IDE connector.
PDCS3#	Primary Slave Chip Select. This signal corresponds to CS3FX# on the primary IDE connector.
PDD [15:0]	Primary Disk Data.
PDIOR#	EIDE Mode: Primary Device I/O Read. Device read strobe. UltraDMA Mode: Primary Host DMA Ready. Primary channel input flow control. The host may assert HDMARDY to pause input transfers Primary Host Strobe. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers
PDIOW#	EIDE Mode: Primary Device I/O Write. Device writes strobe. UltraDMA Mode: Primary Stop. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfers in UltraDMA mode signals the termination of the burst.
PDRDY#	EIDE Mode: Primary I/O Channel Ready. Device ready indicator. UltraDMA Mode: Primary Device DMA Ready. Output flow control. The device may assert DDMARDY to pause output transfers. Primary Device Strobe. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE interface.
IRQ14	Interrupt line from IDE device. Connected directly to PC-AT bus.
PDDRQ	Primary Device DMA Request. Primary channel DMA request.
PDDACK#	Primary Device DMA Acknowledge. Primary channel DMA acknowledges.
PDDACT#	Signal from IDE device indicating IDE device activity. The signal level depends on the IDE device type, normally active low.

2.6.31 CPU Fan Connector (CN12)

Signal	PIN
TAC	3
+12V	2
GND	1

2.6.32 Signal Description – CPU Fan Connector (CN12)

TAC	Fan speed monitor

2.6.33 Front Panel Connector (CN13)

Signal	PIN		Signal
RSTIN	4	8	GND
PWBTI	3	7	GND
GND	2	6	SPK
HD_LED	1	5	VCC

2.6.34 Signal Description – Front Panel Connector (CN13)

HD_LED	IDE device activity signal
PWBTI	Power Button
RSTIN	System Reset
SPK	External Speaker

2.6.35 Floppy Disk Connector (FLP1)

Signal	PIN		Signal
DSKCHG#	34	33	GND
SIDE1#	32	31	GND
RDATA#	30	29	GND
WPT#	28	27	GND
TRAK0#	26	25	GND
WE#	24	23	GND
WD#	22	21	GND
STEP#	20	19	GND
DIR#	18	17	GND
MOB#	16	15	GND
DSA#	14	13	GND
DSB#	12	11	GND
MOA#	10	9	GND
INDEX#	8	7	GND
NC	6	5	GND
NC	4	3	GND
DRVDEN0#	2	1	GND

2.6.36 Signal Description – Floppy Disk Connector (FLP1)

RDATA#	The read data input signal from the FDD.
WD#	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	Write enable. An open drain output.
MOA#	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
MOB#	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DSA#	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSB#	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
SIDE1#	This output signal selects side of the disk in the selected drive.
DIR#	Direction of the head step motor. An open drain output Logic 1 = outward motion Logic 0 = inward motion
STEP#	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
DRVDEN0#	This output indicates whether a low drive density (250/300kbps at low level) or a high drive density (500/1000kbps at high level) has been selected.
TRAK0#	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track.
INDEX#	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole.
WP#	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected.
DSKCHG#	Diskette change. This signal is active low at power on and whenever the diskette is removed.

2.6.37 IrDA Connector (IR1)

Signal	PIN		Signal
NC	2	1	VCC
GND	4	3	IRRX
NC	6	5	IRTX

2.6.38 Signal Configuration – IR Connector (IR1)

IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

2.6.39 10/100 BASE-TX Ethernet Connector (LAN1, LAN2 / ECM-5610 only)

Signal	PIN
NC	8
NC	7
RXD-	6
NC	5
NC	4
RXD+	3
TXD-	2
TXD+	1

2.6.40 Signal Description – 10/100Base-Tx Ethernet Connector (LAN1, LAN2 / ECM-5610 only)

TXD+ / TXD-	Ethernet 10/100Base-Tx differential transmitter outputs.
RXD+ / RXD-	Ethernet 10/100Base-Tx differential receiver inputs.

2.6.41 Panel Link Connector (PL1, Optional)

Signal	PIN		Signal
3.3V	16	15	5V
Txc-	14	13	Txc+
Tx0+	12	11	Tx0-
Tx1+	10	9	Tx1-
Tx2+	8	7	Tx2-
EDGE / HP	6	5	GND
GND	4	3	DDCDAT
DDCCLK	2	1	GND

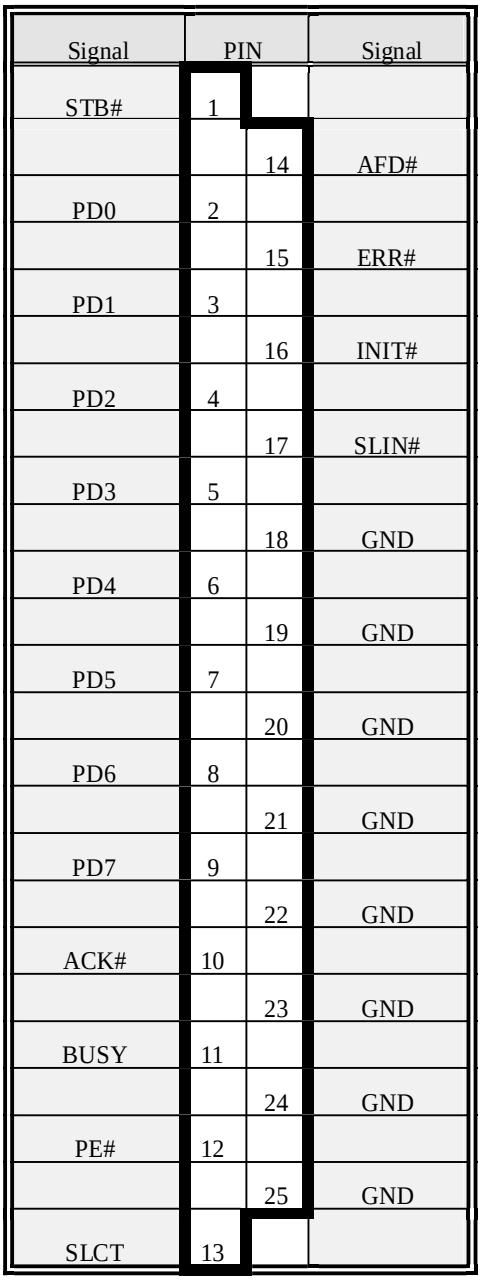
2.6.42 Signal Description – Panel Link Connector (PL1, Optional)

Tx0+, Tx0- Tx1+, Tx1- Tx2+, Tx2-	TMDSTM Low Voltage Differential Signal output data pairs.
Txc+, Txc-	TMDSTM Low Voltage Differential Signal output clock pairs.
EDGE	Edge select / Hot Plug input. If the I2C bus is enabled (ISEL = HIGH), then this pin is used to monitor the "Hot Plug" detect signal (Please refer to the DVITM or VESA® P&DTM and DFP standards). Note: This Input is ONLY 3.3V tolerant and has no internal denouncer circuit. If I2C bus is disabled (ISEL = LOW), then this pin selects the clock edge that will latch the data. How the EDGE setting works depends on whether dual or single edge latching is selected: Dual Edge Mode (DSEL = HIGH) EDGE = LOW, the primary edge (first/even latch edge after DE is asserted) is the falling edge. EDGE = HIGH, the primary edge (first/odd latch edge after DE is asserted) is the rising edge. Note: In 24-bit single clock dual edge mode, EDGE is ignored. Single Edge Mode (DSEL = LOW) EDGE = LOW, the falling edge of the clock is used to latch data. EDGE = HIGH, the rising edge of the clock is used to latch data.
DDCDAT	Dual edge clock select / I2C Data. This pin is an open collector input. If I2C bus is enabled (ISEL = HIGH), then this pin is the I2C data line. If the I2C bus is disabled (ISEL = LOW), then this pin selects whether single clock dual edge is used. Dual edge clock select: When HIGH, IDCK+ latches input data on both falling and rising clock edges. When LOW, IDCK+/IDCK- latches input data on only falling or rising clock edges. In 24-/12-bit mode: If HIGH (dual edge), IDCK+ is used to latch data on both falling and rising edges. If LOW (single edge), IDCK+ latches 1st half data and IDCK- latches 2nd half data.
DDCCLK	Input bus select / I2C clock. This pin is an open collector input. If I2C bus is enabled (ISEL = HIGH), then this pin is the I2C clock input. If the I2C is disabled (ISEL = LOW), then this pin selects the input bus width. Input Bus Select: HIGH selects 24-bit input mode LOW selects 12-bit input mode

2.6.43 Parallel Port Connector (PNT1)

Signal	PIN		Signal
GND	26	25	SLCT
GND	24	23	PE
GND	22	21	BUSY
GND	20	19	ACK#
GND	18	17	PD7
GND	16	15	PD6
GND	14	13	PD5
GND	12	11	PD4
GND	10	9	PD3
SLIN#	8	7	PD2
INIT#	6	5	PD1
ERR#	4	3	PD0
AFD#	2	1	STB#

2.6.44 DB25 Parallel Port Connector



Signal	PIN		Signal
STB#	1		
		14	AFD#
PD0	2		
		15	ERR#
PD1	3		
		16	INIT#
PD2	4		
		17	SLIN#
PD3	5		
		18	GND
PD4	6		
		19	GND
PD5	7		
		20	GND
PD6	8		
		21	GND
PD7	9		
		22	GND
ACK#	10		
		23	GND
BUSY	11		
		24	GND
PE#	12		
		25	GND
SLCT	13		

2.6.45 Signal Description – Parallel Port (PNT1)

The following signal description covers the signal definitions, when the parallel port is operated in standard mode. The parallel port controller also supports the fast EPP and ECP modes.

PD [7:0]	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Output line for detection of printer selection. This pin is pulled high internally.
SLCT	An active high input on this pin indicates that the printer is selected. This pin is pulled high internally.
STB#	An active low output is used to latch the parallel data into the printer. This pin is pulled high internally.
BUSY	An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally.
ACK#	An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally.
INIT#	Output line for the printer initialization. This pin is pulled high internally.
AFD#	An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally.
ERR#	An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally.
PE#	An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally.

2.6.46 USB Connector (USB1)

Signal	PIN CH2	PIN CH1	Signal
VCC2	10	9	GND
D2-	8	7	GND
D2+	6	5	D1+
GND	4	3	D1-
GND	2	1	VCC1

2.6.47 Signal Description – USB Connector (USB1)

D1+ / D1-	Differential bi-directional data signal for USB channel 0. Clock is transmitted along with the data using NRZI encoding. The signaling bit rate is up to 12 Mbs.
D2+ / D2-	Differential bi-directional data signal for USB channel 1. Clock is transmitted along with the data using NRZI encoding. The signaling bit rate is up to 12 Mbs.
VCC	5 V DC supply for external devices. Maximum load according to USB standard.

2.6.48 CRT Connector (VGA1)

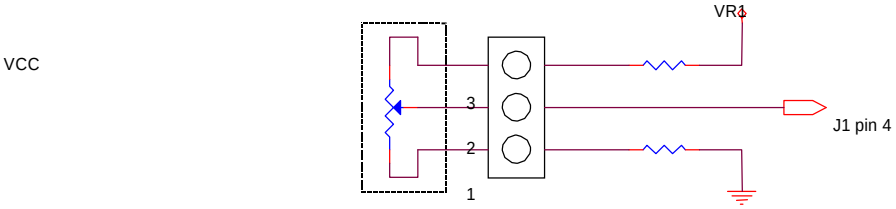
Signal	PIN		Signal
NC	16	8	GND
DDCCLK	15	7	GND
VSYNC	14	6	GND
HSYNC	13	5	GND
DDCDAT	12	4	NC
NC	11	3	BLUE
GND	10	2	GREEN
VCC	9	1	RED

2.6.49 Signal Description – CRT Connector (VGA1)

HSYNC	CRT horizontal synchronization output.
VSYNC	CRT vertical synchronization output.
DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 Ω cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 Ω cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 Ω cable impedance.

2.6.50 LCD Backlight Brightness Adjustment Connector (VR1)

Signal	PIN
VCC	3
VBR	2
GND	1



Variation Resistor (Recommended: 4.7KΩ, >1/16W)

2.6.51 STN LCD Contrast Adjustment Connector (VR2)

Signal	PIN
VCC	3
VCS	2
GND	1

Hardware Configuration Setting

System Installation

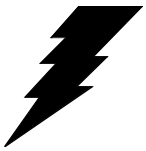
3. System Installation

3.1 Installation Procedure

1. Turn off the power supply.
2. Insert the DIMM module (be careful with the orientation).
3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
4. Connect power supply to the board via the PWR1.
5. Turn on the power.
6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The ***Integrated Peripheral Setup*** and the ***Standard CMOS Setup*** Window must be entered and configured correctly to match the particular system configuration.
7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

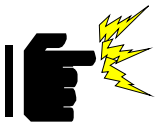
3.2 Safety Precautions

Warning!



Always completely disconnect the power cord from your chassis or power cable from your board whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!



Always ground yourself to remove any static charge before touching the board. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

3.3 Socket 370 Processor

3.3.1 Installing Pentium III / Celeron CPU

- Lift the handling lever of CPU socket outwards and upwards to the other end.
- Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.
- Push down the lever to lock processor chip into the socket.

System Installation

- Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the socket 370.
- Make sure to follow particular CPU speed and voltage type to adjust the jumper settings properly.

Removing CPU

- Unlock the cooling fan first.
- Lift the lever of CPU socket outwards and upwards to the other end.
- Carefully lift up the existing CPU to remove it from the socket.
- Follow the steps of installing a CPU to change to another one or place handling bar back to close the opened socket.

3.3.2 Main Memory

3307246 provides a DIMM socket (168-pin Dual In-line Memory Module) to support 3.3V SDRAM. The maximum memory size is 256MB (registered type of SDRAM). If 133MHz FSB CPU is adopt, you have to use PC-133 compliant SDRAM. For system compatibility and stability, please do not use memory module without brand.

Watch out the contact and lock integrity of memory module with socket, it will influence the system's reliability. Follow the normal procedure to install your SDRAM module into the DIMM socket. Before locking the DIMM module, make sure that the memory module has been completely inserted into the DIMM socket.

System Installation

Note:

Please do not change any SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.

4. AWARD BIOS Setup

4.1 Starting Setup

The Award BIOS™ is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing <Del> immediately after switching the system on, or

By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 To Continue, DEL to enter SETUP

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item in the left hand
Right arrow	Move to the item in the right hand
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu – Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

Table 1: Legend Keys

4.2.1 Navigating Through The Menu Bar

Use the left and right arrow keys to choose the menu you want to be in.

4.2.2 To Display a Sub Menu

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A "¾" pointer marks all sub menus.

4.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

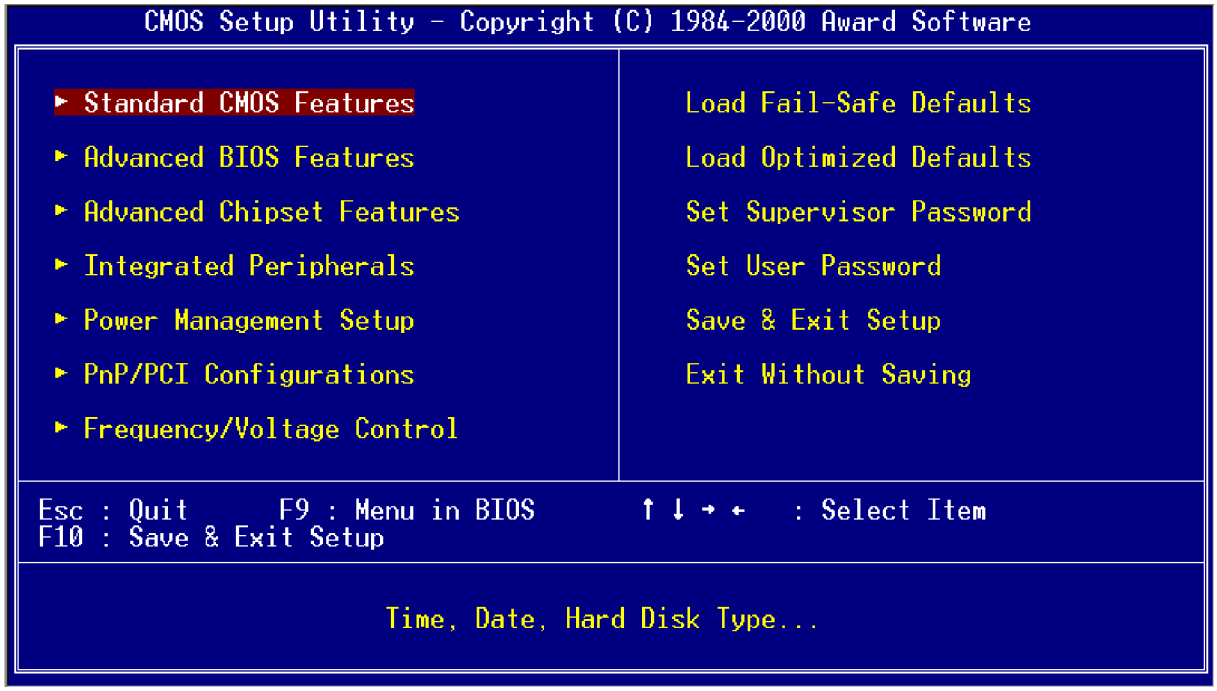
4.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the Award BIOS™ supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings that you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

4.5 Main Menu

Once you enter the Award BIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.



Note that a brief description of each highlighted selection appears at the bottom of the screen.

4.5.1 Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

4.5.1.1 Standard CMOS Features

Use this menu for basic system configuration.

4.5.1.2 Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

4.5.1.3 Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

4.5.1.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

4.5.1.5 Power Management Setup

Use this menu to specify your settings for power management.

4.5.1.6 PNP / PCI Configuration

This entry appears if your system supports PnP / PCI.

4.5.1.7 Frequency / Voltage Control

Use this menu to specify your settings for frequency/voltage control.

4.5.1.8 Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

4.5.1.9 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

4.5.1.10 Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

4.5.1.11 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

4.5.1.12 Exit Without Save

Abandon all CMOS value changes and exit setup.

4.5.2 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into 10 categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

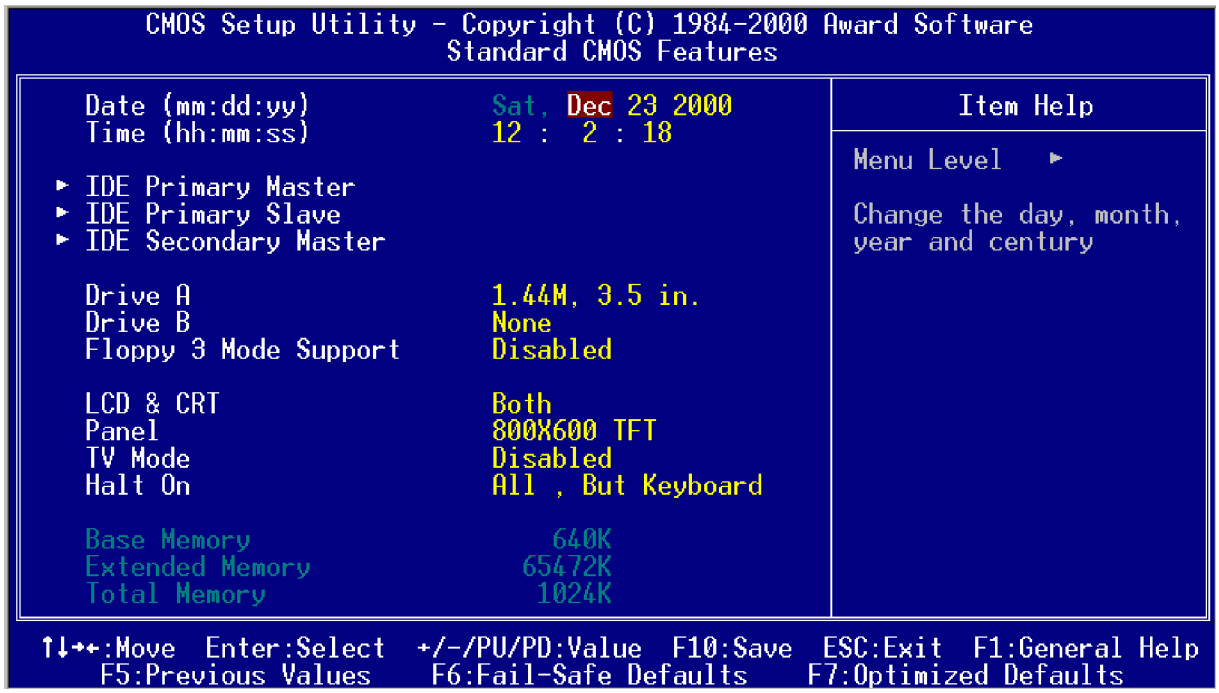


Figure 1: The Main Menu

4.5.2.1 Main Manu Selection

This table shows the selections that you can make on the Main Menu.

Item	Options	Description
Date	Month DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH: MM: SS	Set the system time
IDE Primary Master	Options are in its sub menu (Described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Primary Slave	Options are in its sub menu (Described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (Described in Table 3)	Press <Enter> to enter the sub menu of detailed options
IDE Secondary Master	Options are in its sub menu (Described in Table 3)	Press <Enter> to enter the sub menu of detailed options
Drive A Drive B	None 360K, 5.25 in 1.2M, 5.25 in 720K, 3.5 in 1.44M, 3.5 in 2.88M, 3.5 in	Select the type of floppy disk drive installed in your system
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard All, but Diskette All, but Disk/Key	Select the situation in which you want the BIOS to stop the POST process and notify you
Base Memory	N/A	Displays the amount of conventional memory detected during boot up
Extended Memory	N/A	Displays the amount of extended memory detected during boot up
Total Memory	N/A	Displays the total memory available in the system

Table 2: Main Menu Selections

4.5.2.2 IDE Adapters

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive.

Figure 2 shows the IDE primary master sub menu.

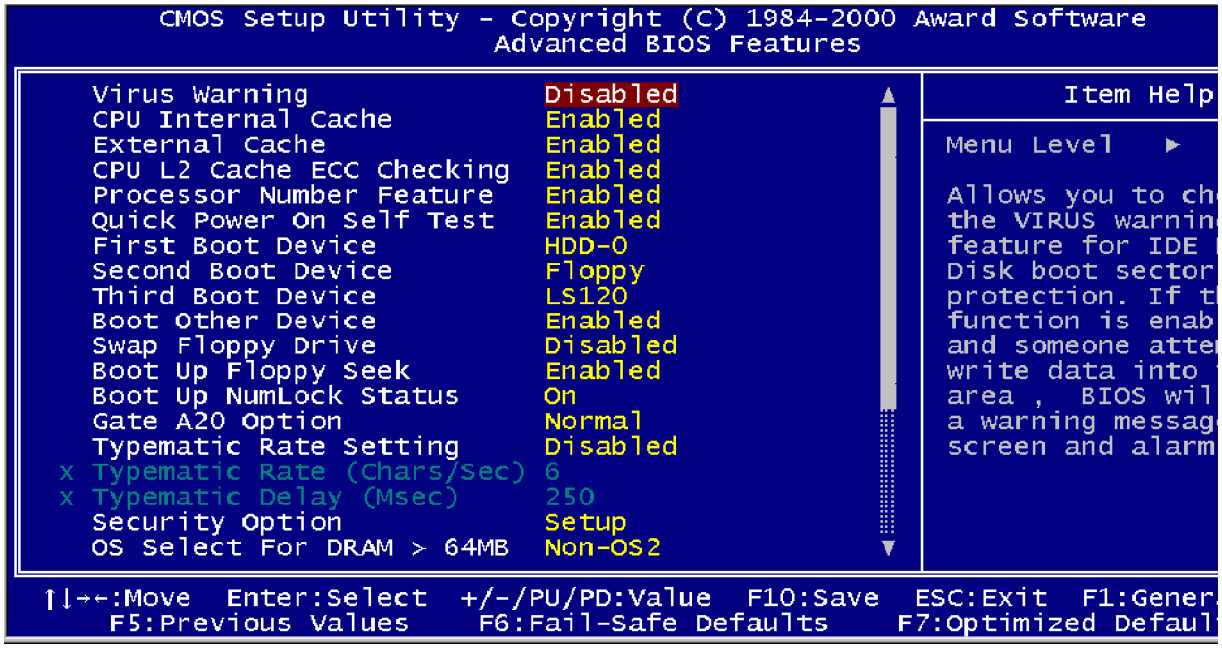
Use the legend keys to navigate through this menu and exit to the main menu. Use Table 3 to configure the hard disk.

Item	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Primary Master	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE!
Capacity	Auto Display your disk drive size	Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Access Mode	Normal LBA Large Auto	Choose the access mode for this hard disk
The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'		
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** **Warning**: Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	****
Sector	Min = 0 Max = 255	Number of sectors per track

Table 3: Hard disk selections

4.5.3 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



4.5.3.1 Virus Warning

Allow you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Enabled	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
Disabled	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

4.5.3.2 CPU Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design.

Enabled	Enable cache
Disabled	Disable cache

4.5.3.3 CPU L2 Cache ECC Checking

This item allows you to enable/disable CPU L2 Cache ECC checking.

The choice: Enabled, Disabled.

4.5.3.4 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.

Enabled	Enable quick POST
Disabled	Normal POST

4.5.3.5 First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the device in the sequence selected in these items.

The Choice: Floppy, LS/ZIP, HDD, SCSI, CDROM, or Disabled.

4.5.3.6 Swap Floppy Drive

If the system has two floppy drives, you can swap the logical drive name assignments.

The choice: Enabled/Disabled.

4.5.3.7 Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.

The choice: Enabled/Disabled.

4.5.3.8 Boot Up NumLock Status

Select power on state for NumLock.

The choice: Enabled/Disabled.

4.5.3.9 Gate A20 Option

Select if chipset or keyboard controller should control GateA20.

Normal	A pin in the keyboard controller controls GateA20
Fast	Lets chipset control GateA20

4.5.3.10 Typematic Rate Setting

Keystrokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

4.5.3.11 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a keystroke when you hold the key down.

The choice: 6, 8, 10, 12, 15, 20, 24, or 30.

4.5.3.12 Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke.

The choice: 250, 500, 750, or 1000.

4.5.3.13 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

4.5.3.14 OS Select for DRAM > 64

Select the operating system that is running with greater than 64MB of RAM on the system.

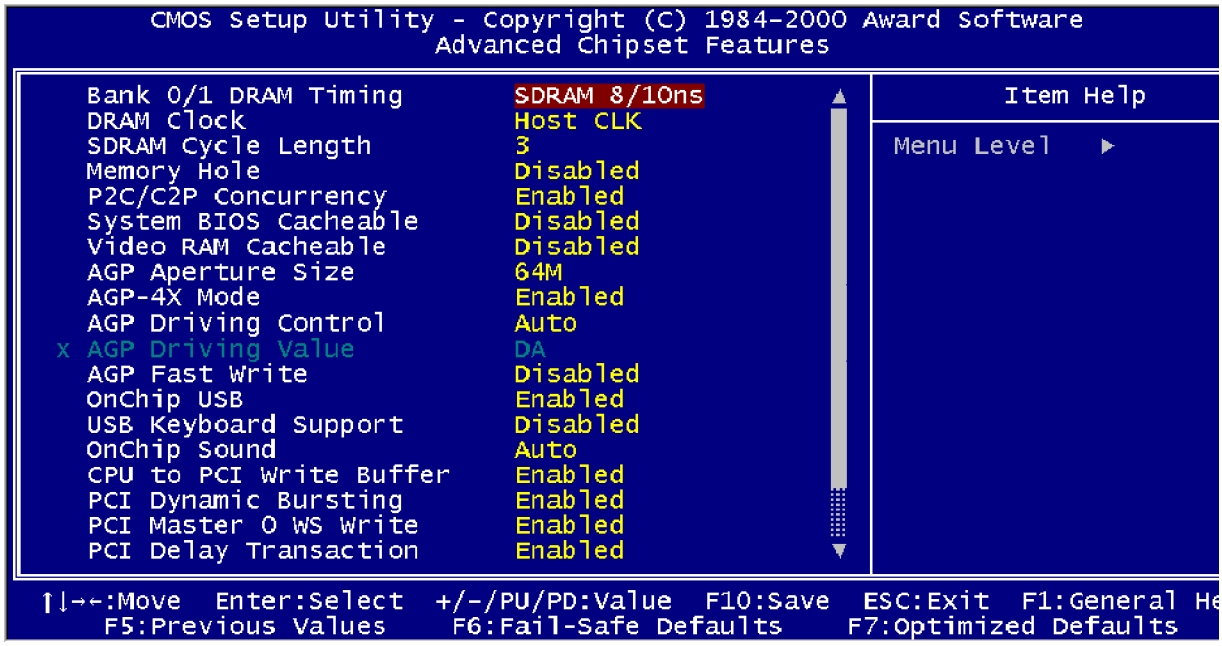
The choice: Non-OS2, OS2.

4.5.3.15 Report No FDD for WIN95

Whether report no FDD for Win 95 or not.

The choice: Yes, No.

4.5.4 Advanced Chipset Features



This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

4.5.4.1 SDRAM Clock Frequency

Set SDRAM clock speed.

The Choice: Auto, 66Mhz.

4.5.4.2 Bank 0/1; Bank 2/3; Bank 4/5 DRAM Timing

This item allows you to select the value in this field, depending on whether the board has paged DRAMs or EDO (extended data output) DRAMs. The choice: from 1 to 16 CPU clocks.

The Choice: 10ns, Normal, Medium, Fast, Turbo.

4.5.4.3 SDRAM Cycle Length

When synchronous DRAM is installed, the number of clock cycles of CAS latency depends on the DRAM timing. Do not reset this field from the default value specified by the system designer.

The Choice: 2, 3.

4.5.4.4 Memory Hole at 15Mb Addr.

In order to improve performance, certain space in memory is reserved for ISA cards. This memory must be mapped into the memory space below 16MB.

The Choice: 15M-16M, Disabled.

4.5.4.5 Read Around Write

DRAM optimization feature: If a memory read is addressed to a location whose latest write is being held in a buffer before being written to memory, the read is satisfied through the buffer contents, and the read is not sent to the DRAM.

The Choice: Enabled, Disabled.

4.5.4.6 Concurrent PCI/Host

When disabled, CPU bus will be occupied during the entire PCI operation period.

The Choice: Enabled, Disabled.

4.5.4.7 System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at F0000h-FFFFFh, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The choice: Enabled, Disabled.

4.5.4.8 Video ROM Cacheable

Select Enabled allows caching of the video RAM, resulting in better system performance. However, if any program writes to this memory area, a system error may result.

The Choice: Enabled, Disabled.

4.5.4.9 Aperture Size

Select the size of Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

The Choice: 4M, 8M, 16M, 32M, 65M, 128M, or 256M.

4.5.4.10 AGP-2X Mode

This item allows you to enable / disable the AGP-2X (Clock 133MHz) Mode.

The Choice: Enabled, Disabled.

4.5.4.11 OnChip USB

This should be enabled if your system has a USB installed on the system board and you wish to use it. Even when so equipped, if you add a higher performance controller, you will need to disable this feature.

The choice: Enabled, Disabled.

4.5.4.12 USB Keyboard Support

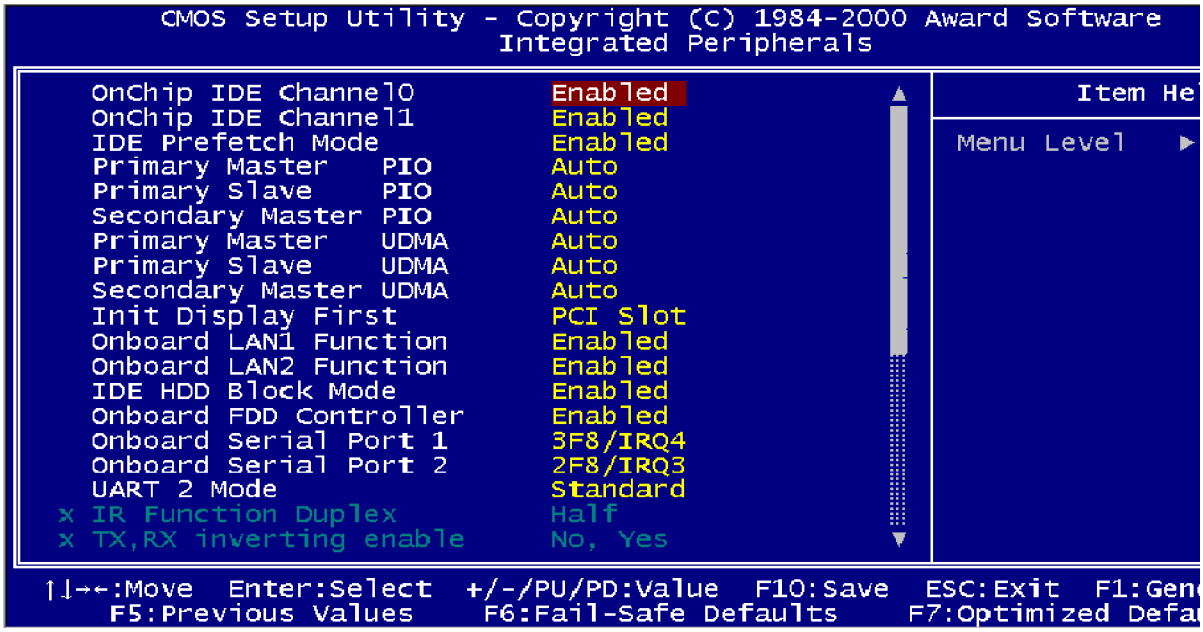
Select *Enabled* if your system contains a Universal Serial Bus (USB) controller and you have a USB keyboard.

The choice: Enabled, Disabled.

4.5.4.13 Memory Parity / ECC Check

This item allows you to select between three methods of memory error checking, Auto, Enabled, and Disabled.

4.5.5 Integrated Peripherals



4.5.5.1 OnChip IDE Channel 0

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.2 OnChip IDE Channel 1

The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the secondary IDE interface. Select Disabled to deactivate this interface.

The choice: Enabled, Disabled.

4.5.5.3 IDE Prefetch Mode

The onboard IDE drive interfaces supports IDE prefetching, for faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to *Disabled* if the interface does not support prefetching.

The choice: Enabled, Disabled.

4.5.5.4 Primary/Secondary Master/Slave PIO

The four IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.

The choice: Auto, Mode 0, Mode 1, Mode 2, Mode 3, or Mode 4.

4.5.5.5 Primary/Secondary Master/Slave UDMA

Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.

The Choice: Auto, Disabled.

4.5.5.6 Init Display First

This item allows you to decide to active whether PCI Slot or AGP first.

The choice: PCI Slot, AGP.

4.5.5.7 Onboard Sound Chip

Select *Enabled* to use the audio capabilities of your system. Most of the following fields do not appear when this field is *Disabled.*

The Choice: Enabled, Disabled.

4.5.5.8 IDE HDD Block Mode

Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

The Choice: Enabled, Disabled.

4.5.5.9 Onboard FDC Controller

Select Enabled if your system has a floppy disk controller (FDC) installed on the system board and you wish to use it. If you install and-in FDC or the system has no floppy drive, select Disabled in this field.

The Choice: Enabled, Disabled.

4.5.5.10 Onboard Serial Port 1/Port2

Select an address and corresponding interrupt for the first and second serial ports.

The choice: 3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto.

4.5.5.11 IR Address Select

Select IR address.

The choice: Disabled, 3F8H, 2F8H, 3E8H, or 2E8H.

4.5.5.12 IR Mode

This item allows you to determine which Infra Red (IR) function of onboard I/O chip.

The Choice: ASKIR, HPSIR.

4.5.5.13 Flat Panel Status

This item allows you to select the option of the build in flat panel controller.

The choice: Enable, Disable.

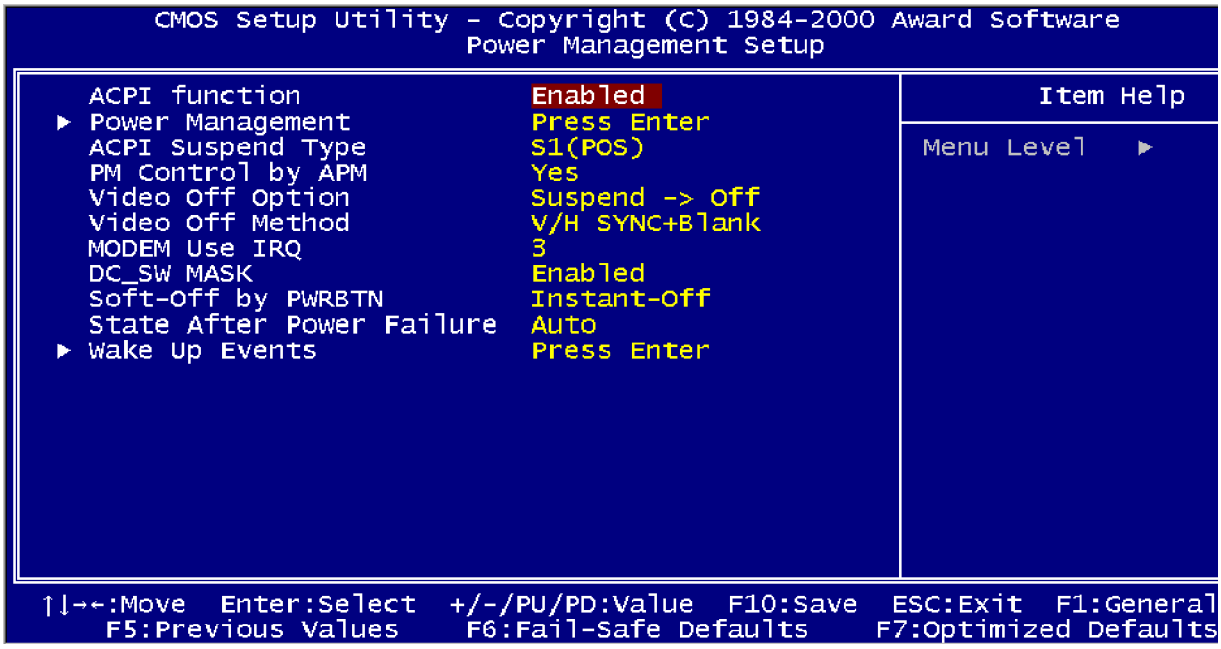
4.5.5.14 Flat Panel Resolution

Select the flat panel resolution.

The choice: 640 x 480, 800 x 600, 1024 x 768.

4.5.6 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.



4.5.6.1 ACPI Function

This item allows you to enable/disable the Advanced Configuration and Power Management (ACPI).

The choice: Enable, Disable.

4.5.6.2 Power Management

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

1. HDD Power Down
2. Doze Mode
3. Suspend Mode

There are four selections for Power Management, three of which have fixed mode settings.

Disable (default)	No power management. Disables all four modes
Min. Power Saving	Minimum power management. Doze Mode = 1 hr. Standby Mode = 1 hr., Suspend Mode = 1 hr., and HDD Power Down = 15 min.
Max. Power Saving	Maximum power management -- **ONLY AVAILABLE FOR SL CPU's**. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min., and HDD Power Down = 1 min.
User Defined	Allow you to set each mode individually. When not disabled, each of the ranges is from 1 min. to 1 hr. except for HDD Power Down, which ranges from 1 min. to 15 min. and disable.

4.5.6.3 PM Control APM

When enabled, an Advanced Power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock.

If the Max. Power Saving is not enabled; this will be preset to *No*.

4.5.6.4 Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank	This selection will cause the system to turn off the vertical and horizontal synchronization ports and write blanks to the video buffer.
Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.

4.5.6.5 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choice: 3, 4, 5, 7, 9, 10, 11, or NA.

4.5.6.6 Soft-Off by PWRBTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".

The choice: Delay 4 Sec, Instant-Off.

4.5.6.7 PM Timers

The following four modes are Green PC power saving functions, which are only user configurable when *User Defined* Power Management has been selected. See above for available selections.

4.5.6.7.1 HDD Power Down

When enabled and after the set time of system inactivity, the hard disk drive will be powered down while all other devices remain active.

4.5.6.7.2 Doze Mode

When enabled and after the set time of system inactivity, the CPU clock will run at slower speed while all other devices still operate at full speed.

4.5.6.7.3 Suspend Mode

When enabled, right after the set time of system inactively, all devices except the CPU will be shut off.

4.5.6.8 PM Events

PM events are I/O events whose occurrence can prevent the system from entering a power saving mode or can awaken the system from such a mode. In effect, the system remains alert for anything, which occurs to a device, which is configured as *On*, even when the system is in a power down mode.

4.5.6.8.1 VGA

When *ON*, your can set the LAN awakens the system.

4.5.6.8.2 LPT & COM

When *select* LPT/COM, any activity from one of the listed system peripheral devices or IRQs wakes up the system.

4.5.6.8.3 HDD & FDD

When *HDD* & FDD is on, any activity from one of the listed system peripheral devices wakes up the system.

4.5.6.8.4 DMA / Master

When you *are On of DMA / ISA Master,* any activity from one of the list system peripheral devices wakes up the system.

4.5.6.8.5 Modem Ring Resume

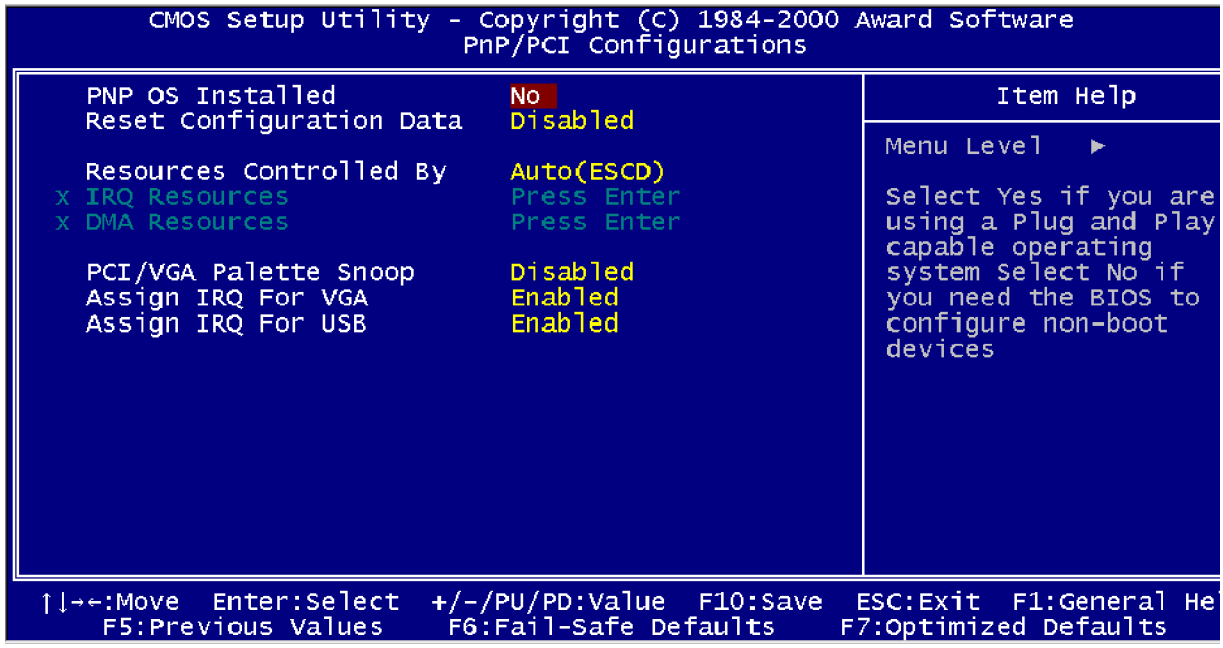
An input signal on the serial Ring Indicator (RI) line (in other words, an incoming call on the modem) awakens the system from a soft off state.

4.5.6.8.6 RTC Alarm Function

When *Enabled*, your can set the date and time at which the RTC (real-time clock) alarm awakens the system from Suspend mode.

4.5.7 PnP/PCI Configuration Setup

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer **I**nterconnect, is a system, which allows I/O devices to operate at speeds nearing the speed the CPU itself, uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.



4.5.7.1 PCI Delay Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

The choice: Enabled, Disabled.

4.5.7.2 PnP OS Installed

This item allows you to determine install PnP OS or not.

The choice: Yes, No.

4.5.7.3 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choice: Enabled, Disabled.

4.5.7.4 Resource Controlled by

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to "manual" choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a "¾").

The choice: Auto, Manual.

4.5.7.5 IRQ Resources

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

4.5.7.6 IRQ3/4/5/7/9/10/11/12/14/15 Assigned to

This item allows you to determine the IRQ assigned to the ISA bus and is not available to any PCI slot. Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

The Choice: *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.7 DMA Resources

When resources are controlled manually, assign each system DMA channel a type, depending on the type of device using the DM channel.

4.5.7.8 DMA 0/1/3/5/6/7 Assigned to

Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture.

Choices are *Legacy ISA* and *PCI/ISA PnP*.

4.5.7.9 Memory Resources

This sub menu can let you control the memory resource.

4.5.7.10 Reserved Memory Base

Reserved a low memory for the legacy device (non-PnP device).

Choices are C800, CC00, D000, D800, DC00, D400, or N/A.

4.5.7.11 Reserved Memory Length

Reserved a low memory length for the legacy device (non-PnP device).

Choices are 8K, 16K, 32K, 64K.

4.5.7.12 PCI / VGA Palette Snoop

Leave this field at *Disabled*.

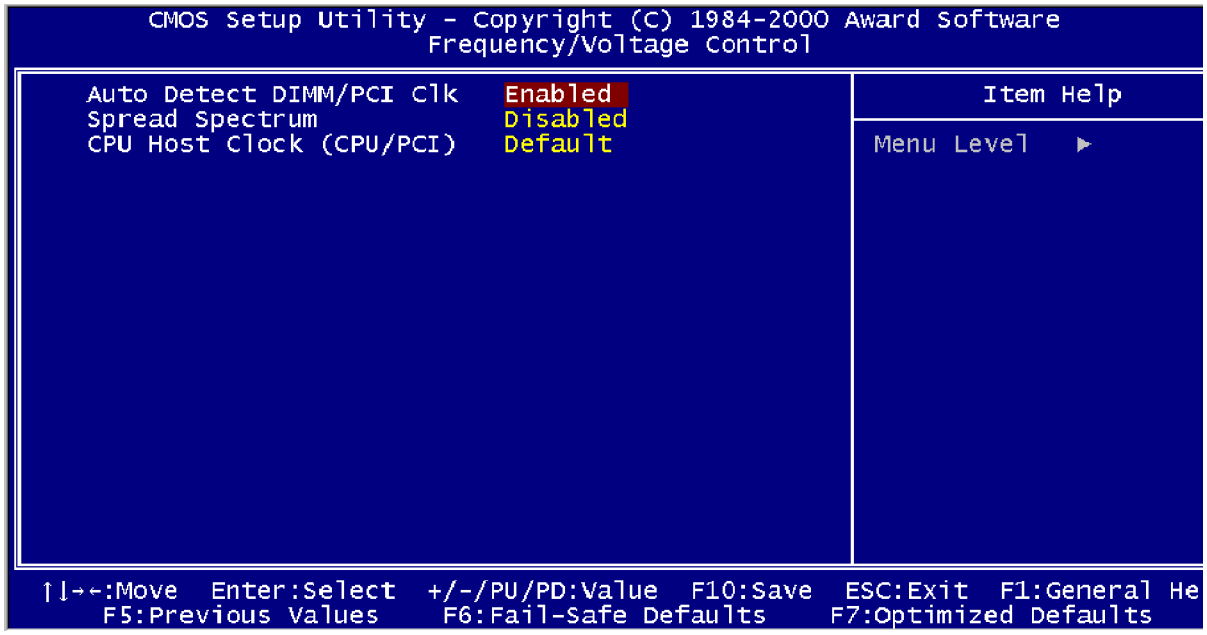
Choices are Enabled, Disabled.

4.5.7.13 Assign IRQ for VGA/USB

Enable/Disable to assign an IRQ for USB/VGA.

Choices are Enabled, Disabled.

4.5.8 Frequency / Voltage Control



4.5.8.1 Auto Detect

This item allows you to enable/disable auto detect DIMM/PCI Clock.

The choice: Enable, Disable.

4.5.8.2 Spread Spectrum Modulated

Spread Spectrum Modulated.

The choice: Enable, Disable.

4.5.8.3 CPU Speed

This item allows you to select the CPU speed.

4.5.8.4 CPU Ratio

This item allows you to select the CPU ratio.

4.5.8.5 CPU Frequency

This item allows you to select the CPU frequency.

4.5.9 Defaults Menu

Selecting "Defaults" from the main menu shows you two options, which are described below.

4.5.9.1 Load Fail-Safe Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load Fail-Safe Defaults (Y/N)? N

Pressing 'Y' loads the BIOS default values for the most stable, minimal-performance system operations.

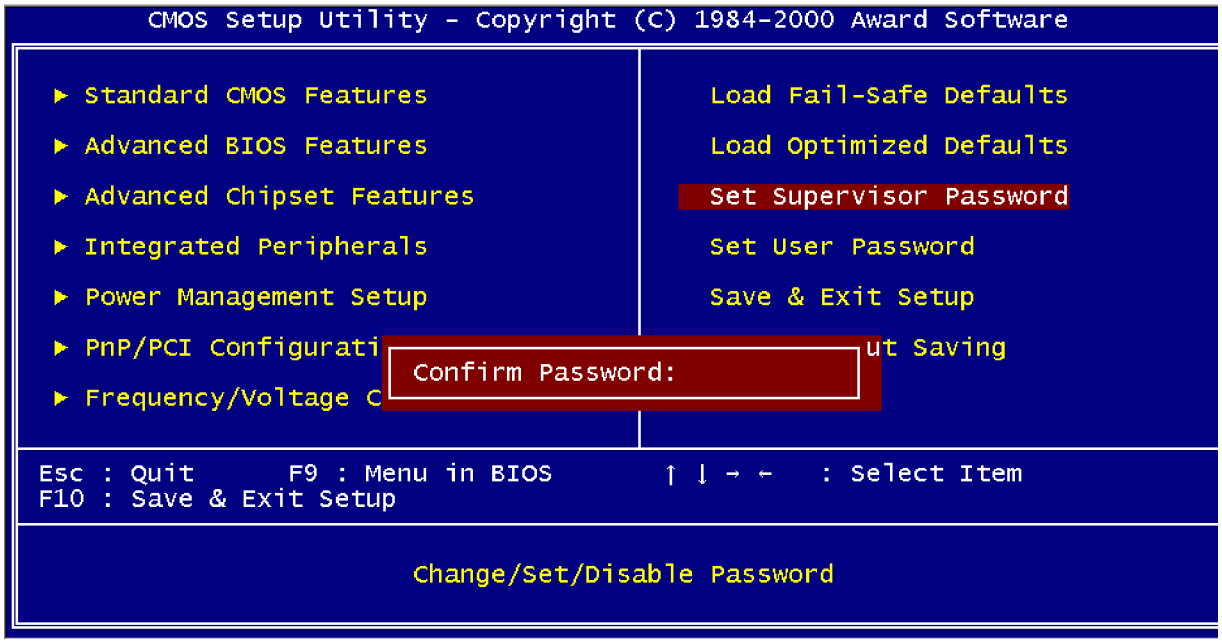
4.5.9.2 Load Optimized Defaults

When you press <Enter> on this item you get a confirmation dialog box with a message similar to:

Load Optimized Defaults (Y/N)? N

Pressing 'Y' loads the default values that are factory settings for optimal performance system operations.

4.5.10 Supervisor / User Password Setting



You can set either supervisor or user password, or both of them. The differences between are:

4.5.10.1 Supervisor password: can enter and change the options of the setup menus.

4.5.10.2 User password: just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the centre of the screen to assist you in creating a password.

ENTER PASSWORD:

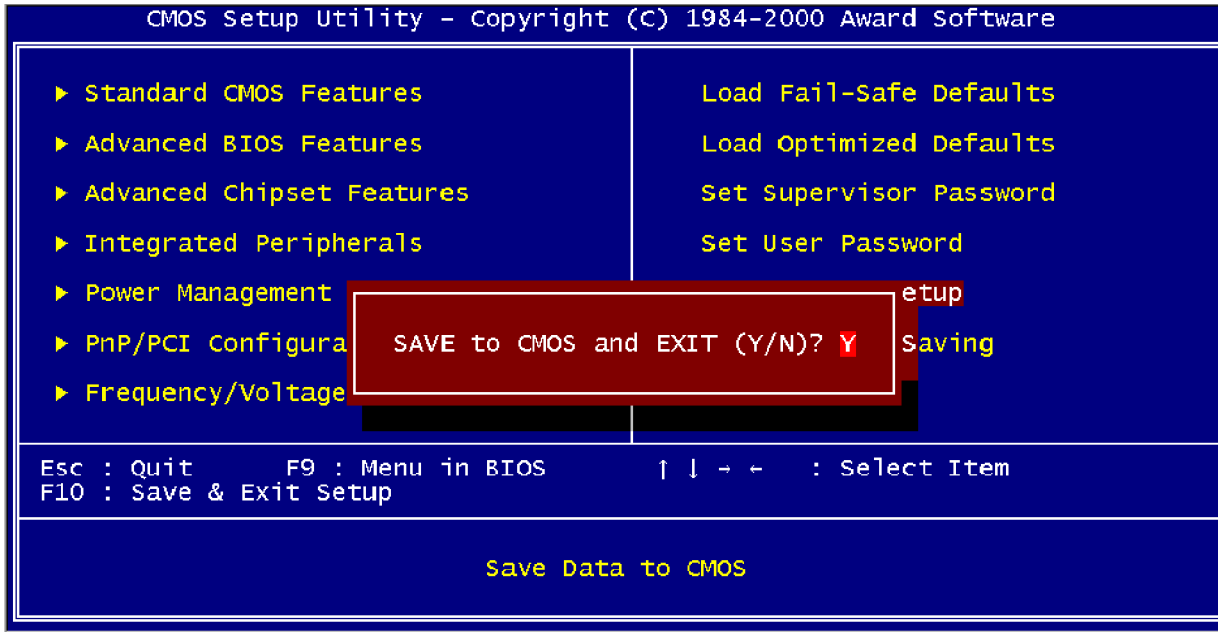
Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If user set to "Setup", prompting only occurs when trying to enter Setup.

4.5.11 Exit Selecting

4.5.11.1 Save & Exit Setup

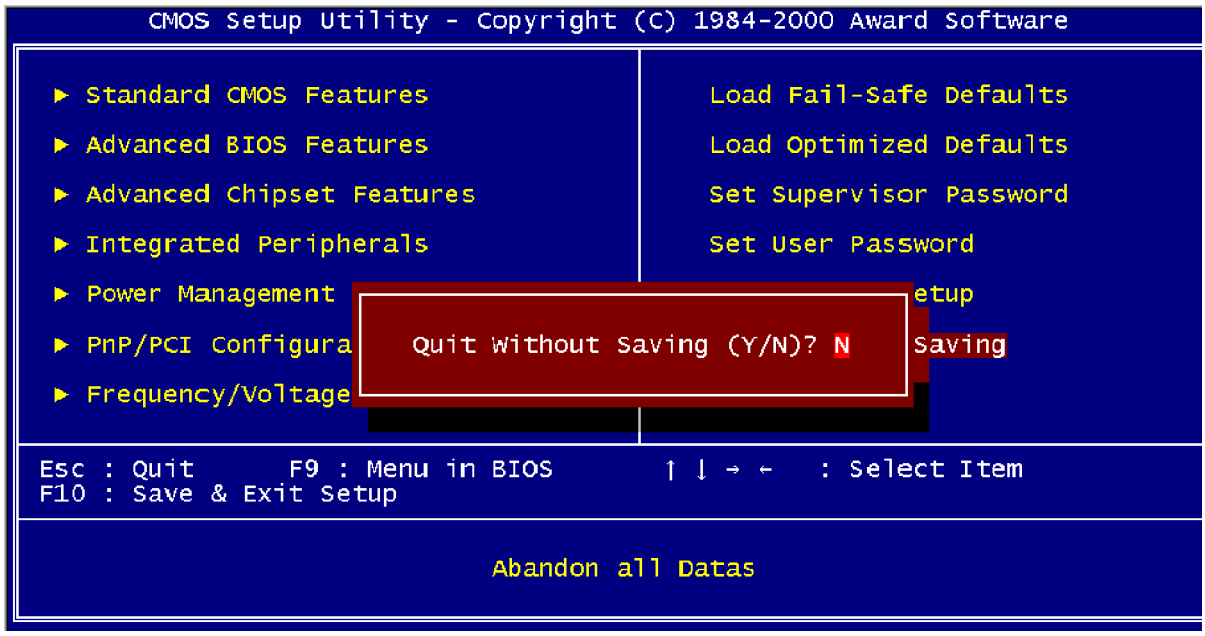


Pressing <Enter> on this item asks for confirmation:

Save to CMOS and EXIT (Y/N)? Y

Pressing "Y" stores the selections made in the menus in CMOS – a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

4.5.11.2 Exit Without Saving



Pressing <Enter> on this item asks for confirmation:

Quit without saving (Y/N)? Y

This allows you to exit Setup without storing in CMOS any change. The previous selections remain in effect. This exits the Setup utility and restarts your computer.

4.6 AWARD BIOS POST Messages

During the Power On Self-Test (POST), if the BIOS detect an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

POST Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detect an error during the POST. This list includes messages for both the ISA and the EISA BIOS

CMOS Battery Has Failed

CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. A weak battery may have caused this error. Check the battery and replace if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error – Run Setup

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

Display Switch Is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

Display Type Has Changed Since Last Boot

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

Error Encountered Initialising Hard Drive

Hard drive cannot be initialised. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

Error Initialising Hard Disk Controller

Cannot initialise controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy Disk Cntrlr Error or No Cntrlr Present

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there is no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

Keyboard Error or No Keyboard Present

Cannot initialise the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

Memory Address Error at...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error at...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

Memory Verify Error at...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address Not Found

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

Offending Segment:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

Press A Key to Reboot

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

Press F1 to Disable NMI, F2 to Reboot

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error – Checking for Segment...

Indicates a parity error in Random Access Memory.

System Halted, (CTRL-ALT-DEL) to Reboot...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

Floppy Disk(s) Fail (80) ⟶ Unable to Reset Floppy Subsystem

Floppy Disk(s) Fail (40) ⟶ Floppy Type Mismatch

Hard Disk(s) Fail (80) ⟶ HDD Reset Failed

Hard Disk(s) Fail (40) ⟶ HDD Controller Diagnostics Failed

Hard Disk(s) Fail (20) ⟶ HDD Initialisation Error

Hard Disk(s) Fail (10) ⟶ Unable to Recalibrate Fixed Disk

Hard Disk(s) Fail (08) ⟶ Sector Verify Failed

Keyboard Is Locked Out - Unlock The Key

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

Manufacturing POST Loop

System will repeat POST procedure infinitely while the P15 of keyboard controller is pulled low. This is also used for M/B burn in test.

BIOS ROM Checksum Error – System Halted

The checksum of ROM address F0000H-FFFFFH is bad.

Memory Test Fail

BIOS reports the memory test fails if the onboard memory is tested error.

4.7 AWARD BIOS POST Codes

POST Code (hex)	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)

POST Code (hex)	Description
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detects ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the Run time area in F000 for ESCD & DMI support.
11h	Reserved

POST Code (hex)	Description
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial Early_Init_Onboard_Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead. 3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information. 4. Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 5. Early PCI initialization: -Enumerate PCI bus number -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0.
24h	Reserved

POST Code (hex)	Description
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer

POST Code (hex)	Description
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	Reserved
2Bh	Reserved
2Ch	Reserved
2Dh	1. Initialize multi-language 2. Put information on screen display, including Award title, CPU type, and CPU speed ….
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.

POST Code (hex)	Description
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program writes allocation for AMD K5 CPU.

POST Code (hex)	Description
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO switch. 2. Initialize Init_Onbaord_AUDIO switch.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved

POST Code (hex)	Description
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h

POST Code (hex)	Description
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved
73h	(Optional Feature) Enter AWDFLASH.EXE if : -AWDFLASH is found in floppy drive. -ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
7Fh	1. Switch back to text mode if full screen logo is supported. -If errors occur, report errors & wait for keys -If no errors occur or F1 key is pressed to continue: Š Clear EPA or customization logo.
80h	Reserved
81h	Reserved

POST Code (hex)	Description
82h	1. Call chipset power management hook
	2. Recover the text fond used by EPA logo (not for full screen logo)
	3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
POST Code (hex)	**Description**
85h	1. USB final Initialization 2. NET PC: Build SYSID structure 3. Switch screen back to text mode
	4. Set up ACPI table at top of memory. 5. Invoke ISA adapter ROMs 6. Assign IRQs to PCI devices 7. Initialize APM 8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program boot up speed 3. Chipset final initialization. 4. Power management final initialization 5. Clear screen & display summary table 6. Program K6 write allocation 7. Program P6 class write combining
95h	1. Program daylight saving 2. Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support you for your products, projects and business

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