User's Manual

Industrial PC-based Automation

3307346

Full-size PICMG Socket 370 Pentium III / Celeron PC-133 CPU Card with 4xAGP SVGA, Fast Ethernet Interface and DiskOnChipSocket

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Trademarks

Part number : 4011631300120

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Introduction

The SBC is based on VIA's ProSavage™ PL133 that combine PC-133, 133MHz FSB, UltraDMA/100 IDE technologies and rich 4xAGP 2D/3D graphics capabilities in a single package. Its onboard 10Base-T/100Base-TX Fast Ethernet, CRT display controller, optional AC'97 3D Audio and TMDS Panel Link LCD Interfaces add communication and multimedia features to its powerfull function.

A wide range of CPUs including Intel® Pentium® III/ Celeron™ and VIA Cyrix® III processors are supported up to 1GHz at 133MHz FSB, while memory is expandable to 1.5GB PC-133 SDRAM.

The VIA ProSavage™ PL133 dual-chipset consists of the VT8604 Northbridge and VT82C686B Super Southbridge. It integrates VIA Apollo Pro133A chipset with 4xAGP 32MB S3® Savage4™ and S3® Savage2000™ 2D graphics core.

The highlight of the Super Southbridge supports high speed PCI UltraDMA/100 enhanced IDE which can tremendously increases transfer speed for database applications. Other exclusive features include onboard DiskOnChip®+ 2000 socket for memory up to 288MB.

Specifications

General Specifications

- CPU : Socket 370 FC-PGA/PPGA Pentium®III, Celeron™, VIA C3™ with 133/100/66MHz FSB
- Chipset : VIA ProSavage™ PL133 (VT8604 Northbridge and VT82C686B "Super" Southbridge) integrates VIA Apollo Pro133A, S3® Savage4™ 3D and S3® Savage2000™ 2D engines and supports PC-133 memory bus, 133MHz FSB and UltraATA/100 IDE interfaces
- BIOS : AWARD® Flash BIOS Green&Soft Off function, LS120, multiple boot function
- Green Function : power saving supported in BIOS. DOZE /STANDBY / SUSPEND modes, ACPI & APM
- L2 Cache : Integrated on CPU
- DRAM Memory : up to 1.5GB of SDRAM in three 168-pin DIMM sockets (supports PC-133 SDRAM)
- PCI Enhanced IDE with UltraDMA : supports 2 ports and up to 4 ATAPI devices. UltraDMA transfer 33/66 and 100 MB/sec
- Watchdog Timer : 127-level timer generates RESET or NMI when your application loses control over the system.
- Real-time Clock : built-in chipset with lithium battery backup for 10 years of data retention. CMOS data backup of BIOS setup and BIOS default.

High Speed Multi I/O

- Chipset : included in VT82C686B "Super" Southbridge
- Serial Ports : one external high speed RS-232C port COM1 (DB9 on bracket), one internal high speed RS-232C/422/485 port COM2 (jumper selectable, 10-pin box header). Both with 16C550 compatible UART and 16 byte FIFO.
- USB : 4 onboard USB ver 1.0 ports (Dual 2x 5-pin header)
- SIR Interface : onboard IrDA TX/RX port (5-pin header)
- Floppy Disk Drive Interface : 2 floppy disk drives, 5¼" (360 KB or 1.2 MB) and 3½" (720 KB, 1.44 MB or 2.88 MB).
- Bi-directional Parallel Port : SPP, EPP and ECP mode.
- Keyboard and Mouse Connectors : external PS/2 KB/Mouse port (2-in-1 mini DIN) onboard AT Keyboard port (5-pin box header)

Network Interface Controller

- Chipset : RTL8139C, 10/100 Mbps, autoswitching
- Connector : external RJ-45 with LEDs on bracket

Audio Interface (Optinal)

- Connector : 16-pin header for Audio daughterboard
- Audio Daughterboard : Soundblaster Pro and Direct Sound Ready AC97 Digital Audio controller. LINE-in/out CD-in, Mic-in and stereo speakers.

Display Controller

- Chipset : 4x AGP S3® Savage4™ 3D and S3® Savage 2000™ 2D engines integrated in VT8604 Supports up to 32MB shared SDRAM
- Display Type : CRT (VGA, SVGA, XGA, SXGA) LCD (optional, see LCD Daughterboard)
- Connectors : external DB15 for CRT on bracket and 42-pin header for TMDS daughterboard
- LCD Display Daughterboard (optional) : TMDS Panel Link with DVI interface and 20-pin connector for LCD monitor

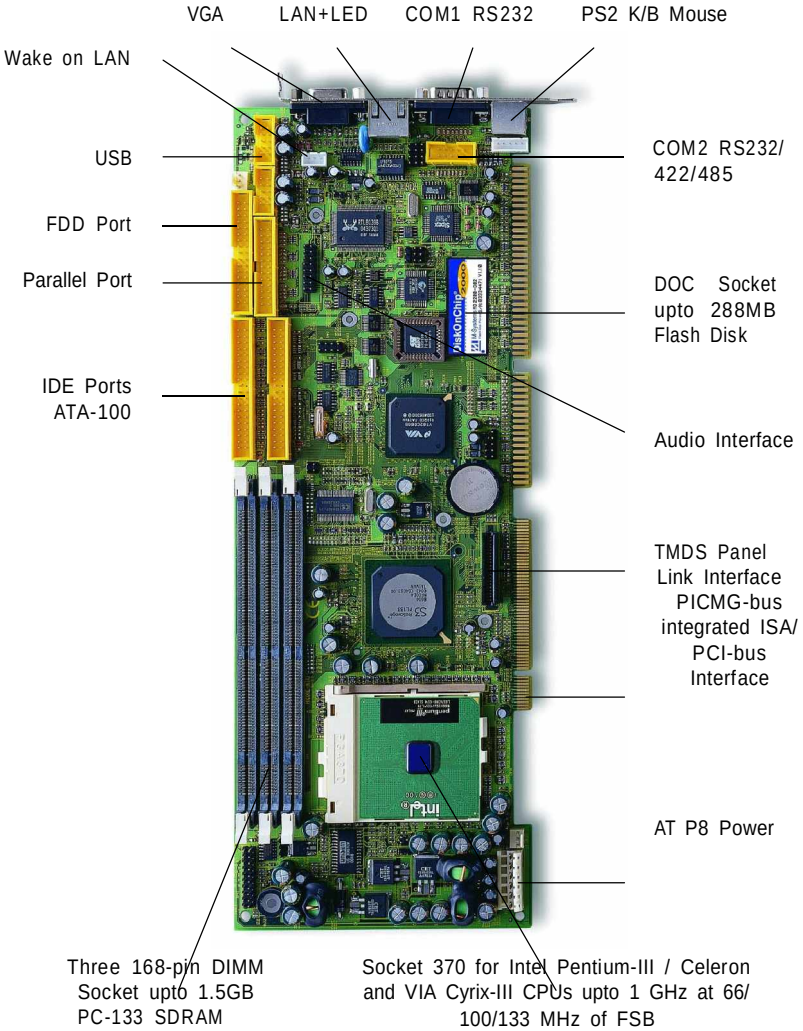
Flash Disk DiskOnChip®2000

- Package : Single Chip Flash Disk in 32-pin DIP JEDEC
- Capacity : up to 288 MByte
- Data Reliability : ECC/EDC error correction
- Memory Window : 8 KByte

Environmental and Power

- Power Requirements : +5 V @ 4.2 A (typical), ±12 V ; (FC-PGA Pentium® III 800 MHz at 133 FSB and 256 MB PC-133 SDRAM)
- CPU Power : onboard PWM switching power supply for autodetects CPU core voltage
- System Monitoring and Alarm : CPU and System temperature, system voltage and cooling fan RPM.
- Board Dimensions : 338 mm x 122 mm
- Board Weight : 0.45 Kg.
- Operating Temperature : 0 to 60°C (32 to 140°F)

Component Location



Warning

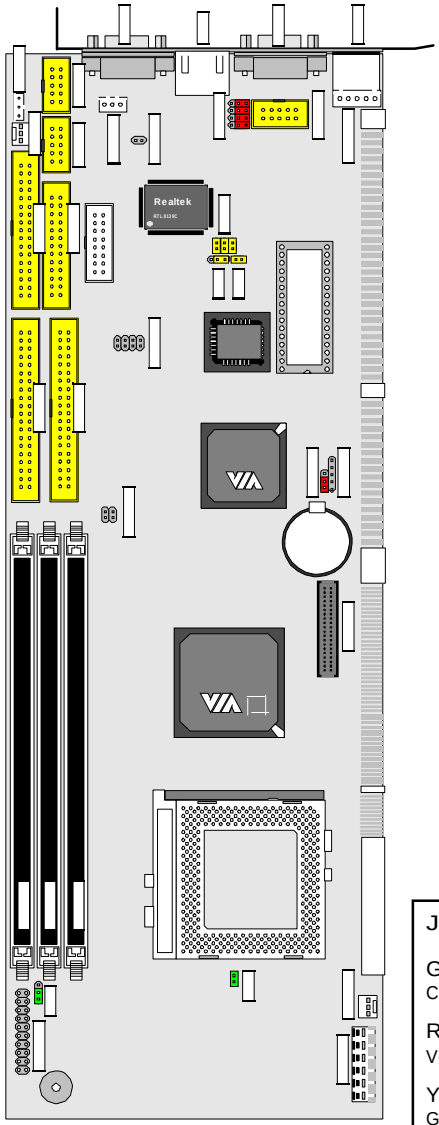
Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system

Ordering Codes

3307346		Full-size PICMG-bus Socket 370 Pentium-III / Celeron PC-133 CPU Card with 4xAGP 3D SVGA, Fast Ethernet, Optional 3D Audio Interface and DiskOn-Chip® Socket
3901140	:	TMDS Daughterboard with 20-pin LCD Monitor Cable Kit
3507345	:	AC97 3D Audio Daughterboard with Cable Kit

Board Layout Front



Jumper Colors

Green :
CPU Speed Ratio

Red :
Voltage Settings

Yellow :
General configuration

Jumper/Connector Quick Reference

Jumpers

J1/J4 CPU Type Selection

CPU type	J1	J4
Intel PPGA	2-3	OFF
Intel FC-PGA	2-3	ON
VIA C3 (Old)	1-2	OFF

SW2 CPU Host Clock Ratio

7-8	5-6	3-4	1-2	Ratio
ON	ON	ON	ON	2.0
ON	OFF	ON	ON	2.5
ON	ON	OFF	ON	3.0
ON	OFF	OFF	ON	3.5
ON	ON	ON	OFF	4.0
ON	OFF	ON	OFF	4.5
ON	ON	OFF	OFF	5.0
ON	OFF	OFF	OFF	5.5
OFF	ON	ON	ON	6.0
OFF	OFF	ON	ON	6.5
OFF	ON	OFF	ON	7.0
OFF	OFF	OFF	ON	7.5
OFF	ON	ON	OFF	8.0
OFF	OFF	OFF	OFF	Auto

SW1 FSB Speed Selection

1-2	3-4	Ratio
OFF	OFF	133 Mhz / Auto
OFF	ON	100 Mhz
ON	ON	66 MHz

JBAT CMOS Operation

1-2	->	Normal Operation
2-3	->	Clear CMOS

J6 DiskOnChip Base Address

ON	->	D0000h
OFF	->	D8000h

J5 Watchdog Active Mode

1-2	->	active NMI
2-3	->	System RESET
OFF	->	Disabled

JV1~JV4 COM1(2) RS-232 Mode

SW3 COM2 RS-232/422/485 Mode

COM2 Mode

J2 LAN Function

ON	->	Disable
OFF	->	Enable

Connectors

CPUF1	CPU Fan Power
SYSF1	System Fan Power
JLCD1	Flat Panel Module
JIR1	IrDA Header
ATKB1	internal AT Keyboard
COM1	COM 1 on bracket
KB1	PS/2 Mouse / Keyboard
J3	RJ-45 LAN on bracket
VGA1	CRT SVGA on bracket
COM2	COM2 in RS-232 mode
WOL1	Wake On LAN
ATX1	ATX Signal Connector
FDD1	FDD interface
LPT1	LPT1, Parallel PORT
IDE1	Primary IDE
IDE2	Secondary IDE
JAMR1	Audio Module Connector
USB1	Primary/Secondary USB
USB2	3rd / 4th USB
JFRT1	Front Panel Header

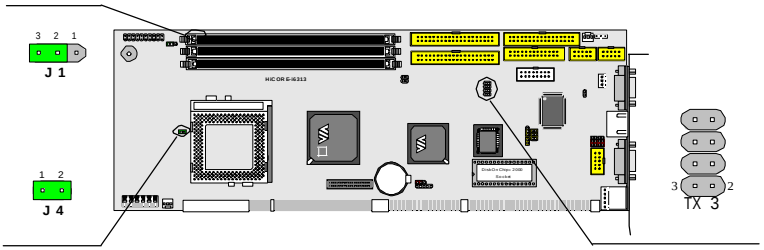
CPU and CMOS Jumper Settings

CPU Type Selector

Connector : J1, J4
Type : J1: onboard 3-pin header; J4: onboard 2-pin header

CPU Type	J1	J4
Intel PPGA Celeron	2-3	OFF
Intel FC-PGA Pentium III / Celeron, VIA C3 Ezra / Matthew	2-3	ON
VIA C3 Joshua / Samuel 1/2	1-2	OFF

default setting



CPU Host Clock Ratio Selector

Connector : SW2
Type : onboard 8-pin header

Ratio	SW2			
	7-8	5-6	3-4	1-2
2.0	ON	ON	ON	ON
2.5	ON	OFF	ON	ON
3.0	ON	ON	OFF	ON
3.5	ON	OFF	OFF	ON
4.0	ON	ON	ON	OFF
4.5	ON	OFF	ON	OFF
5.0	ON	ON	OFF	OFF
5.5	ON	OFF	OFF	OFF
6.0	OFF	ON	ON	ON
6.5	OFF	OFF	ON	ON
7.0	OFF	ON	OFF	ON
7.5	OFF	OFF	OFF	ON
8.0	OFF	ON	ON	OFF
Auto	OFF	OFF	OFF	OFF

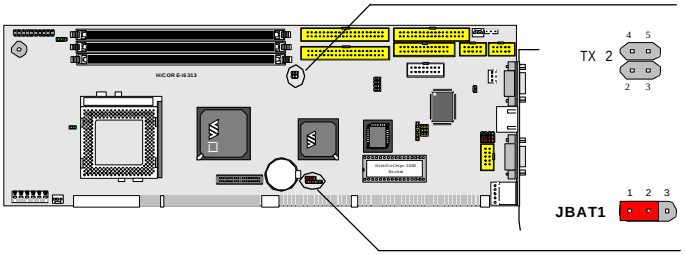
default setting

CPU FSB Speed Selector

Connector : SW1
Type : onboard 4-pin header

SW1	1-2	3-4
133MHz/Auto	OFF	OFF
100MHz	OFF	ON
66MHz	ON	ON

default setting



CMOS Operation

If the SBC refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values

Connector:JBAT1
Type:onboard 3-pin header

Mode	JBAT1
Normal Operation	1-2
Clear CMOS	2-3

default setting

Watchdog Timer

The onboard watchdog timer can be disable by jumper setting or enable for either reboot by system RESET or invoking an NMI (Non-Maskable Interrupt)

Even if enabled by jumper setting upon boot the watchdog timer is always inactive. To initialize or refresh the watchdog timer writing of port 444h is sufficient. To disable the watchdog time read port 44h.

Status	Action
Enable/refresh the Watchdog Timer	I/O Write 444H
Disable the Watchdog Timer.	I/O Read 44H

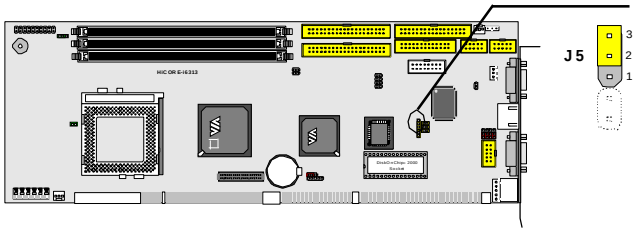
After the watchdog timer has been initialized by writing port 444h, it has to be strobed at preconfigured intervals to keep it from issuing a RESET or NMI.

The watchdog timer timeout intervals are set by software programming.

Mode Setting

Watchdog Mode	J5
Enabled for Active NMI(I/O Channel Check)	1-2
Enabled for System Reset	2-3
Disable Watchdog Timer	None

default setting



Timeout Values

Timout values are programmed. The watchdog timer supports 127 steps. use the table on the next page to find the hexidecimal value that needs to be passed on to get the correct timer interval. Look subsequntly at the program example how to pass the value to the watchdog timer.

Timeout Table

Level	Value	Seconds	Level	Value	Seconds	Level	Value	Seconds
1	7Fh	1	2	7Eh	2	3	7Dh	3
4	7Ch	4	5	7Bh	5	6	7Ah	6
7	79h	7	8	78h	8	9	77h	9
10	76h	10	11	75h	11	12	74h	12
13	73h	13	14	72h	14	15	71h	15
16	70h	16	17	6Fh	17	18	6Eh	18
19	6Dh	19	20	6Ch	20	21	6Bh	21
22	6Ah	22	23	69h	23	24	68h	24
25	67h	25	26	66h	26	27	65h	27
28	64h	28	29	63h	29	30	62h	30
31	61h	31	32	60h	32	33	5Fh	33
34	5Eh	34	35	5Dh	35	36	5Ch	36
37	5Bh	37	38	5Ah	38	39	59h	39
40	58h	40	41	57h	41	42	56h	42
43	55h	43	44	54h	44	45	53h	45
46	52h	46	47	51h	47	48	50h	48
49	4Fh	49	50	4Eh	50	51	4Dh	51
52	4Ch	52	53	4Bh	53	54	4Ah	54
55	49h	55	56	48h	56	57	47h	57
58	46h	58	59	45h	59	60	44h	60
61	43h	61	62	42h	62	63	41h	63
64	40h	64	65	3Fh	65	66	3Eh	66
67	3Dh	67	68	3Ch	68	69	3Bh	69
70	3Ah	70	71	39h	71	72	38h	72
73	37h	73	74	36h	74	75	35h	75
76	34h	76	77	33h	77	78	32h	78
79	31h	79	80	30h	80	81	2Fh	81
82	2Eh	82	83	2Dh	83	84	2Ch	84
85	2Bh	85	86	2Ah	86	87	29h	87
88	28h	88	89	27h	89	90	26h	90
91	25h	91	92	24h	92	93	23h	93
94	22h	94	95	21h	95	96	20h	96
97	1Fh	97	98	1Eh	98	99	1Dh	99
100	1Ch	100	101	1Bh	101	102	1Ah	102
103	19h	103	104	18h	104	105	17h	105
106	16h	106	107	15h	107	108	14h	108
109	13h	109	110	12h	110	111	11h	111
112	10h	112	113	0Fh	113	114	0Eh	114
115	0Dh	115	116	0Ch	116	117	0Bh	117
118	0Ah	118	119	09h	119	120	08h	120
121	07h	121	122	06h	122	123	05h	123
124	04h	124	125	03h	125	126	02h	126
127	01h	127						

Programming Example

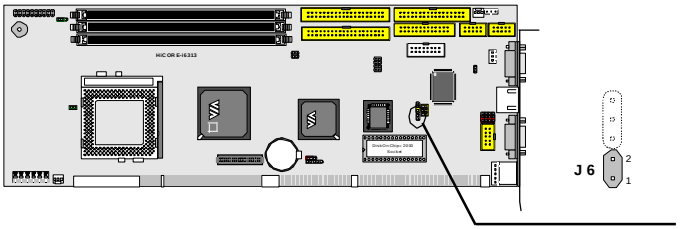
The following program is an examples of how to enable, disable and refresh the Watchdog timer:

```
WDT_EN_RF     equ    444h

WDT_DIS       equ    044h

WT_Enable     push  AX              ;  Save  AX,DX
              push  DX
              mov  DX,WDT_EN_RF     ;  Enable  Timer
              mov  AX,INTERVAL      ;  Set  Timeout  Value
              out  DX,AX
              pop  DX               ;  Restore  DX,AX
              pop  AX
              ret

WT_Refresh    push  AX              ;  Save  AX,DX
              push  DX
              mov  DX,WDT_EN_RF     ;  Refresh  Timer
              mov  AX,INTERVAL      ;  Set  Timout  Value
              out  DX,AX
              pop  DX               ;  Restore  DX,AX
              pop  AX
              ret

WT_Disable    push  AX              ;  Save  AX,DX
              push  DX
              mov  DX,WDT_DIS       ;  Disable  Timer
              in  AX,DX
              pop  DX               ;  Restore  DX,AX
              pop  AX
              ret

WT_Disable    push  AX              ;  save  AX,DX
              push  DX
              mov  DX,WDT_DIS       ;  Disable  Timer
              in  AX,DX
              pop  DX               ;  restore  DX,AX
              pop  AX
              ret
```

DiskOnChip® 2000 Flash Disk

Installation Instructions

1. Make sure the Single Board Computer is powered OFF.
2. Plug the DOC (DiskOnChip®2000) device into its socket. Verify the direction is correct (pin 1 of the DiskOnChip®2000 is aligned with pin 1 of the socket)



3. Set address

Base Address	J6
D8000h	OFF
D0000h	ON

default setting

4. Power up the system
5. During power up you may observe a message displayed by the DOC when its drivers are automatically loaded into system's memory
6. At this stage the DOC can be accessed as any disk in the system
7. If the DOC is the only disk in the system, it will appear as the first disk (drive C: in DOS)
8. If there are more disks besides the DOC, the DOC will appear by default as the last drive, unless it was programmed as first drive. (please refer to the DOC utilities user manual)
9. If you want the DOC to be bootable:
   a - copy the operating system files into the DOC by using the standard DOS command (for example: sys d:)
   b - The DOC should be the only disk in the systems or should be configured as the first disk in the system (c:) using the DUPDATE utility

For more information on DiskOnChip®2000, visit M-Systems Web site at

http:// www.m-sys.com

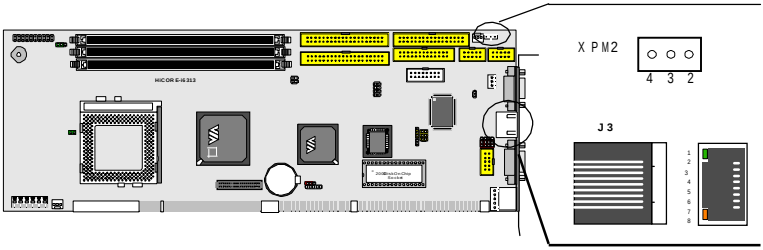
where you can find the utilities manual, data sheets and application notes. In addition, you can find the latest DiskOnChip®2000 S/W utilities.

Single Chip Fast Ethernet Controller

LAN Port

Connector : J3
Type : external RJ-45 on bracket

Pin	1	2	3	4	5	6	7	8
Desciption	TX+	TX-	RX+	NC	NC	RX-	NC	NC



LAN LED Indicator on RJ-45 connector

Connector : LED
Type : 2 LED

LED	ACT (yellow)	Speed (green)
Desciption	Active Transfer	100 MB mode

Wake On LAN

Connector: WOL1
Type : onboard 3-pin wafer connector

Pin	Description
1	5V_SB
2	GND
3	WOL_CTL

LAN Function Enable / Disable

Connector : J2
Type : onboard 2-pin header

LAN Function	J2
Enable	OFF
Disable	ON

default setting

Serial Port Selection (RS232C/422/485)

RS-232c Standard and POS Modes

The onboard COM1 and COM2 ports can be configured to operate in standard RS-232C mode or in POS (Point-of-Sale) RS-232C mode. POS devices normally need an additional power supply signal (+5V or 12V) to be able to power the serial devices (LCD, cash drawer, scanner, touch screen or printer) without additional wiring.

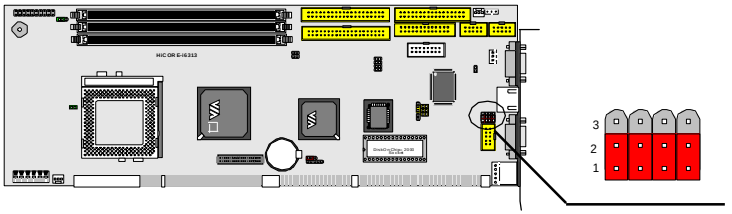
There are three seperate POS modes :
- RS-232 with 5V on pin 1
- RS-232 with 12V on pin 9
- RS-232 with 5V on pin 1 and 12V on pin 9

POS modes are configured by JV1/JV2 for COM1 and JV3/JV4 for COM2

NOTE : in RS-232 mode COM1 is assigned to external connector COM1
COM2 is assigned to onboard connector COM2

COM1 RS-232 Mode	JV1	JV2
Standard	1-2	1-2
POS : 5V on pin 1	2-3	1-2
POS : 12V on pin 9	1-2	2-3
POS : 5V on pin 1 and 12V on pin 9	2-3	2-3

default setting

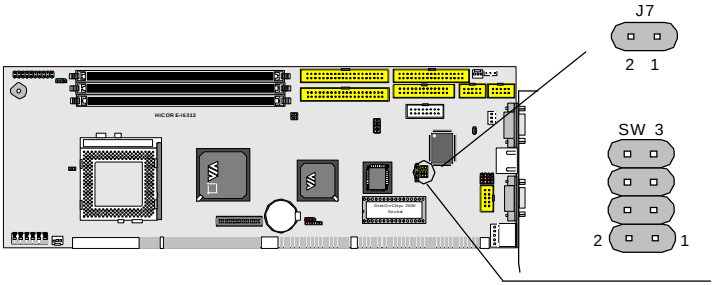


COM2 RS-232 Mode	JV3	JV4
Standard	1-2	1-2
POS : 5V on pin 1	1-2	2-3
POS : 12V on pin 9	2-3	1-2
POS : 5V on pin 1 and 12V on pin 9	2-3	2-3

default setting

RS-422/485 Mode on COM2

The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper SW3 switches between RS-232 or RS-422/485 mode. When SW3 is set to RS-422 or 485 mode, there will be only +12V output left while JV4 is set. All of the RS-232/422/485 modes are available on COM2.



SW3 Mode Selection	1-2	3-4	5-6	7-8	J7
RS-232	OFF	OFF	OFF	OFF	ON
RS-422	OFF	OFF	OFF	OFF	OFF
RS-485	ON	ON	ON	ON	OFF

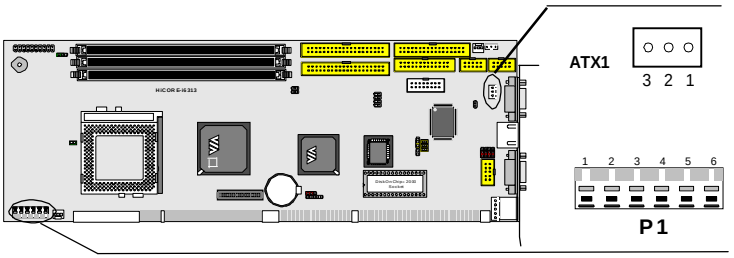
default setting

Power Connectors

Power Connectors

Connector : P1
Type : 6-pin onboard AT P8 Connetor

Pin	Description
1	PWR_GOOD
2	VCC
3	+12V
4	-12V
5	GND
6	GND



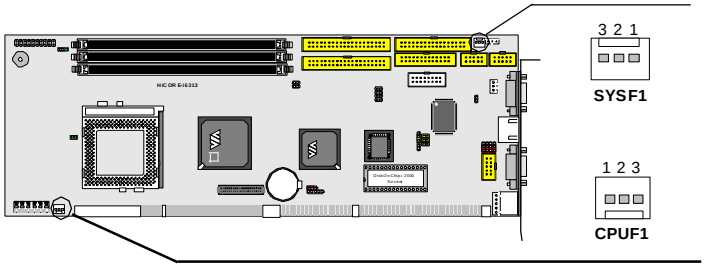
Connector : ATX1
Type : onboard 3-pin Wafer connector

Pin	Description
1	5V SB(Standby)
2	GND
3	PS-ON

CPU Fan Connector

Connector : CPUF1
Type : onboard 3-pin wafer connector

Pin	Description
1	GND
2	+12V
3	FAN_CTL

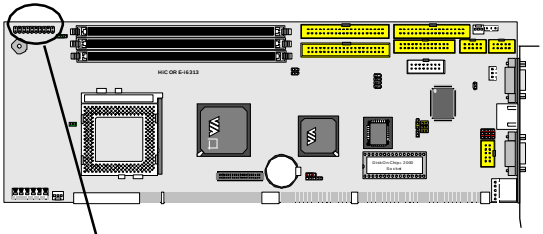


Chassis Auxilary Fan Connector

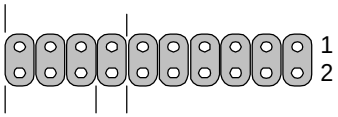
Connector : SYSF1
Type : onboard 3-pin header

Pin	Description
1	GND
2	+12V
3	FAN_CTL

Switches and Indicators

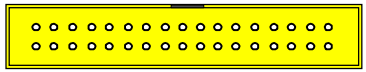


JFRT1



Interface Connectors HDD, FDD

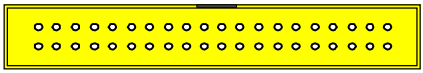
Floppy Disk Drive Connector



Connector : FDD1
Type : onboard 34-pin box header

Pin	Description	Pin	Description
1	GND	2	DRIVE DENSITY SELECT 0
3	GND	4	DRIVE DENSITY SELECT 1
5	GND	6	NC
7	GND	8	INDEX-
9	GND	10	MOTOR ENABLE A-
11	GND	12	DRIVER SELECT B-
13	GND	14	DRIVER SELECT A-
15	GND	16	MOTOR ENABLE B-
17	GND	18	DIRECTION-
19	GND	20	STEP-
21	GND	22	WRITE DATA-
23	GND	24	WRITE GATE-
25	GND	26	TRACK 0-
27	GND	28	WRITE PROTECT-
29	GND	30	READ DATA-
31	GND	32	HEAD SELECT-
33	GND	34	DISK CHANGE-

Enhanced IDE Connector

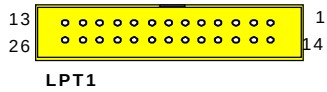


Connector : IDE1 and IDE2
Type : Two onboard 40-pin box headers, primary and secondary IDE

Pin	Description	Pin	Description
1	RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N C
21	REQ	22	GND
23	IOW-/STOP	24	GND
25	IOR-/HDMARDY	26	GND
27	IORDY/DDMARDY	28	IDESEL
29	DACK-	30	GND
31	IRQ	32	N C
33	A1	34	CBLID
35	A0	36	A2
37	CS0(MASTER CS)	38	CS1(SLAVE CS)
39	LED ACT-	40	GND

Peripheral Ports

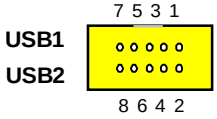
Parallel Port



Connector : LPT1
Type : onboard 26-pin box header

Pin	Description	Pin	Description
1	STROBE-	14	AUTO FEED-
2	DATA0	15	ERROR-
3	DATA1	16	INITIALIZE-
4	DATA2	17	SELECT INPUT-
5	DATA3	18	GND
6	DATA4	19	GND
7	DATA5	20	GND
8	DATA6	21	GND
9	DATA7	22	GND
10	ACKNOWLEDGE-	23	GND
11	BUSY	24	GND
12	PAPER EMPTY	25	GND
13	SELECT+	26	N/C

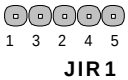
USB Ports



Connector: USB1, USB2
Type:onboard 10-pin box header for four USB ports

Pin	**Description**	**Pin**	**Description**
1	VCC	2	VCC
3	DATA	4	DATA
5	DATA	6	DATA
7	GND	8	GND
9	GND	10	GND

IrDA

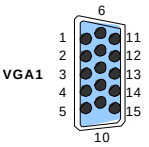


Connector : JIR1
Type : onboard 5-pin header

Pin	Description	Pin	Description
1	Vcc	2	NC
3	IRRX	4	GND
5	IRTX		

CRT SVGA

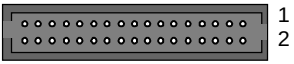
Connector : VGA1
Type : external 15-pin D-sub female connector on bracket



Pin	Description	Pin	Description	Pin	Description
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	VDDAT
3	BLUE	8	GND	13	HSYNC
4	NC	9	Vcc	14	VSYNC
5	GND	10	GND	15	VDCLK

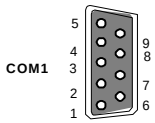
TMDS LCD / External TV Encoder Port

Connector:JLCD1
Type:onboard 42-pin box header



Pin	Description	Pin	Description
1	PCIRST-	2	GND
3	USB_DT3+	4	USB_DT3-
5	GND	6	OC0(USB Over-Current)
7	VCC	8	GND
9	GND	10	VCC3
11	VCC	12	GND
13	GND	14	VCC3
15	FP_D11/TV_BLANK	16	GND
17	FP_DET/TV_D11	18	SPD1(Serial Port Data)
19	FP_D10/TV_D10	20	GND
21	FP_D9/TV_D9	22	SPCLK1(Serial Port Clock)
23	FP_D8/TV_D8	24	GND
25	FP_D7/TV_D7	26	GOP0
27	FP_D6/TV_D6	28	GND
29	FP_D5/TV_D5	30	FP_DEN/TV_CLK
31	FP_D4/TV_D4	32	GND
33	FP_D3/TV_D3	34	FP_CLK/TV_CLKR
35	FP_D2/TV_D2	36	GND
37	FP_D1/TV_D1	38	FP_VS/TV_VS(VSYNC)
39	FP_D0/TV_D0	40	GND
41	GND	42	FP_HS/TV_HS(HSYNC)

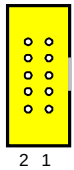
COM1 RS-232C Ports on bracket



Connector : COM1
Type : external 9-pin D-sub male connector on bracket

Pin	Description	Pin	Description
1	DCD (or POS mode +5V)	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI (or POS mode +12V)		

COM2 with RS-232C Mode



Connector : COM2
Type : onboard 10-pin box header

Pin	Description	Pin	Description
1	DCD (or POS mode +5V)	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI (or POS mode +12V)	10	NC

COM2 with RS-422/485 Mode

Connector : COM2
Type : onboard 10-pin box header

RS-422 Mode

Pin	Description	Pin	Description
1	TXN	2	TXP
3	RXP	4	RXN
5	GND	6	NC
7	NC	8	NC
9	NC	10	NC

RS-485 Mode

Data- of RS-485 is connected by pin-1

Data+ of RS-485 is connected by pin-2

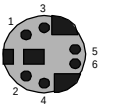
AT Keyboard

Connector : ATKB1
Type : Onboard 5-pin header

Pin	Description	Pin	Description
1	CLK	2	DATA
3	NC	4	GND
5	NC		

Note: ATKB1doesn't provide Vcc power pin on pin-5, that is, ATKB1 cannot connect to AT keyboard directly. ATBK1 supports AT keyboard with passive backplane.

PS/2 Keyboard & Mouse



Connector: KB1
Type: external 6-pin Mini DIN connector on bracket

	Pin	Description	Pin	Description
	1	KB-DATA	2	MS-DATA
	3	GND	4	VCC
	5	KB-CLK	6	MS-CLK

Note: KB1 supports PS/2 keyboard directly, and PS/2 mouse suppoted with the additional PS2 1-to-2 cable in the standard packing.

AC97 Audio Interface Port

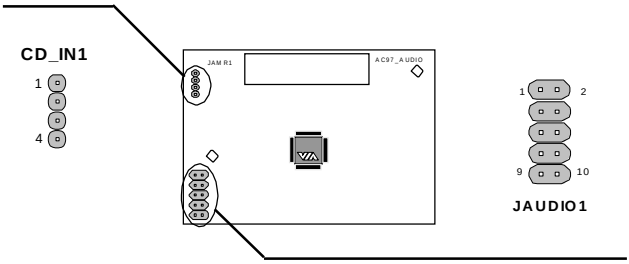
Connector:JAMR1
Type:onboard 16-pin box header

Pin	Description	Pin	Description
1	GND	2	GND
3	GND	4	SDIN2(AC97 Serial Data In 2)
5	VCC	6	SDINA(AC97 Serial Data In)
7	VCC3	8	BITCLK_A(AC97 Bit Clock)
9	3V3_SB	10	ACRST-(AC97 Reset)
11	5V_SB	12	SPEAK
13	-12V	14	SYNC(AC97 Sync)
15	+12V	16	SDOUT(AC97 Serial Data Out)

Interface Daughter Board

AC97 3D Audio Codec Daughter Board (Optional) (3507345)

This daughter board connects to JAMR1 of SBC.



Connector : CD_IN1
Type : Onboard 4-pin header

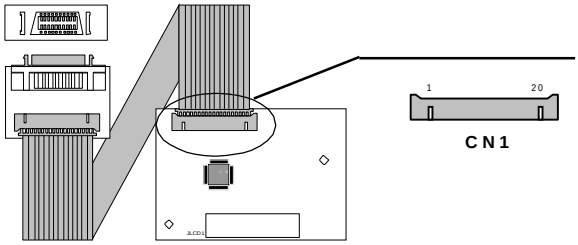
Pin	Description	Pin	Description
1	CD_Left	2	GND
3	GND	4	CD_Right

Connector : JAUDIO1
Type : Onboard 10-pin header

Pin	Description	Pin	Description
1	Line in_Left	2	Line in_Right
3	GND	4	GND
5	MIC_IN	6	VDD
7	GND	8	GND
9	Line out_Left	10	Line out_Right

TMDS Panel Link Daughter Board (Optional) (3901140)

This daughter board connects to JLCD1 of SBC.



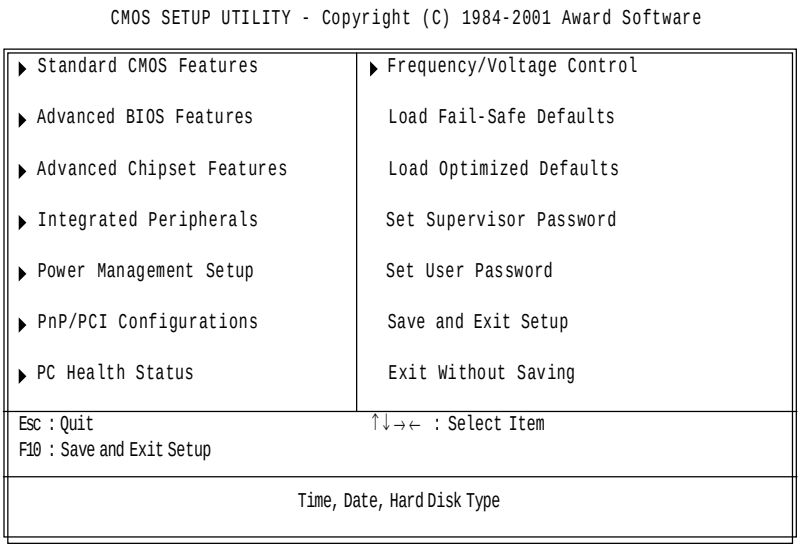
Connector : CN1
Type : Onboard 20-pin header

Pin	Description	Pin	Description
1	VCC	11	FP AGND
2	FP AGND	12	TXC+
3	TX2+	13	TXC-
4	TX2-	14	FP AGND
5	FP AGND	15	USBDT+
6	TX1+	16	USBDT-
7	TX1-	17	FP AGND
8	FP AGND	18	SPCLK1
9	TX0+	19	SPD1
10	TX0-	20	FPDET

AWARD BIOS Setup

The SBC uses the Award PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press <Del> key. The Main Menu will be displayed at this time.



Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

Standard CMOS Features
Use this menu for basic system configuration.

Advanced BIOS Features
Use this menu to set the Advanced Features available on your system.

Advanced Chipset Features
Use this menu to change the values in the chipset registers and optimize your system's performance.

Integrated Peripherals
Use this menu to specify your settings for integrated peripherals.

Power Management Setup
Use this menu to specify your settings for power management.

PnP / PCI Configuration
This entry appears if your system supports PnP / PCI.

Frequency/Voltage Control
Use this menu to specify your settings for frequency/voltage control.

Load Fail-Safe Defaults
Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

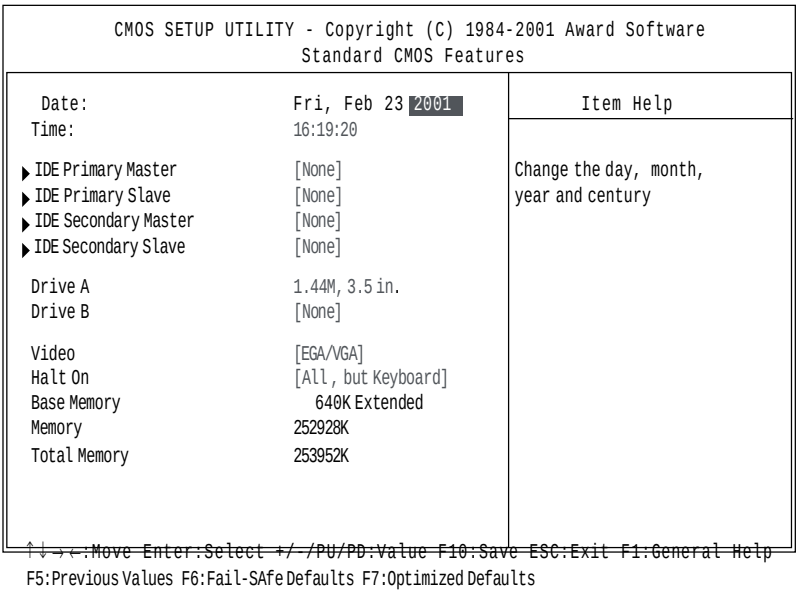
Load Optimized Defaults
Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

Supervisor / User Password
Use this menu to set User and Supervisor Passwords.

Save & Exit Setup
Save CMOS value changes to CMOS and exit setup.

Exit Without Save
Abandon all CMOS value changes and exit setup.

Standard CMOS Setup



Date

The BIOS determines the day of the week from the other date information; this field is for information only.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field . Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

IDE Primary Master/Slave
IDE Secondary Master/Slave

Options are in sub menu (see page 30)

Drive A, B

Select the correct specifications for the diskette drive(s) installed in the computer.

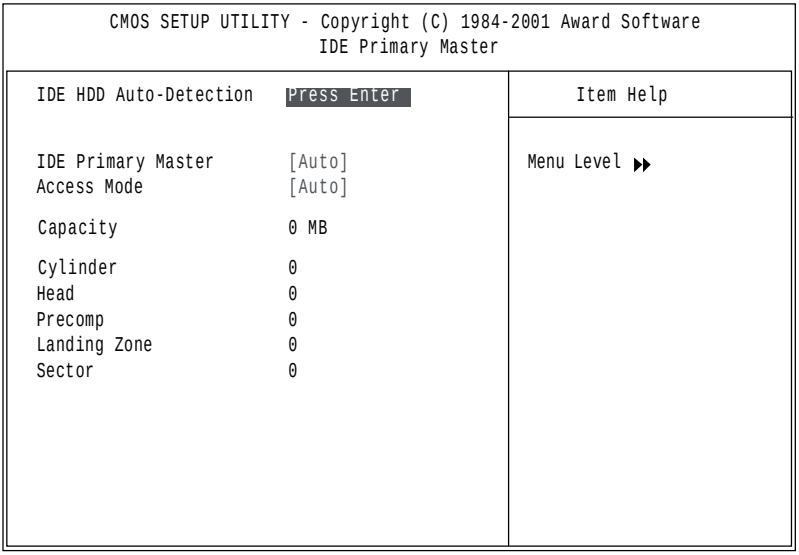
None :	No diskette drive installed
360K ;	5.25 in 5-1/4 inch PC-type standard drive
1.2M ;	5.25 in 5-1/4 inch AT-type high-density drive
720K ;	3.5 in 3-1/2 inch double-sided drive
1.44M ;	3.5 in 3-1/2 inch double-sided drive
2.88M ;	3.5 in 3-1/2 inch double-sided drive

Video Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but you do not select it in Setup.

Halt On During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections:

No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

IDE Harddisk Setup (submenu)



IDE HDD Auto-detection
Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.

IDE Primary Master
Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !

Capacity
Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.

Access Mode
Normal, LBA, Large or Auto Choose the access mode for this hard disk

The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder Min = 0 Max = 65535
Set the number of cylinders for this hard disk.

Head Min = 0 Max = 255
Set the number of read/write heads

Precomp Min = 0 Max = 65535
**** Warning: Setting a value of 65535 means no hard disk

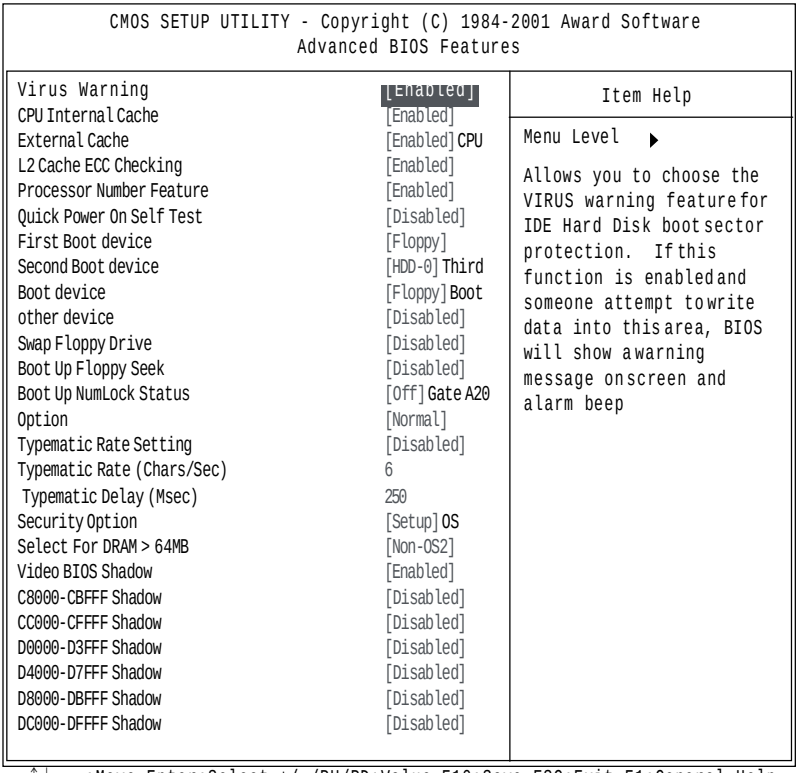
Landing zone Min = 0 Max = 65535
**** Warning: Setting a value of 65535 means no hard disk

Sector Min = 0 Max = 255
Number of sectors per track

We recommend that you select Type "AUTO" for all drives. The BIOS will auto-detect the hard disk drive and CD-ROM drive at the POST stage.

If your hard disk drive is a SCSI device, please select "None" for your hard drive setting.

BIOS Features Setup



Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and beep.

Enabled Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.

Disabled No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

CPU Internal Cache/External Cache
These two categories speed up memory access. However, it depends on CPU/chipset design. Enabled : Enable cache, Disabled : Disable cache

CPU L2 Cache ECC Checking
This item allows you to enable/disable CPU L2 Cache ECC checking.
The choice: Enabled, Disabled.

Processor Number Feature
This feature appears when a a Pentium III processor is installed. It enables you enables you to control whether the Pentium III's serial number can be read by external programs. The choice : Enabled. Disabled

Quick Power On Self Test
This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST. Enabled : Enable quick POST. Disabled : Normal POST

First/Second/Third/Other Boot Device
The BIOS attempts to load the operating system from the devices in the sequence selected in these items. The choices are : Floppy, LS/ZIP, HDD, SCSI, CDROM, Disabled.

Swap Floppy Drive
If the system has two floppy drives, you can swap the logical drive name assignments. The choice: Enabled/Disabled.

Boot Up Floppy Seek
Seeks disk drives during boot up. Disabling speeds boot up.
The choice: Enabled/Disabled.

Boot Up NumLock Status
Select power on state for NumLock. The choice: Enabled/Disabled.

Gate A20 Option
Select if chipset or keyboard controller should control GateA20.
Normal A pin in the keyboard controller controls GateA20
Fast Lets chipset control GateA20

Typematic Rate Setting
Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.
The choice: Enabled/Disabled.

Typematic Rate (Chars/Sec)
Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

Typematic Delay (Msec)
Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

Security Option
Select whether the password is required every time the system boots or only when you enter setup.

System The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

Setup The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

Note To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

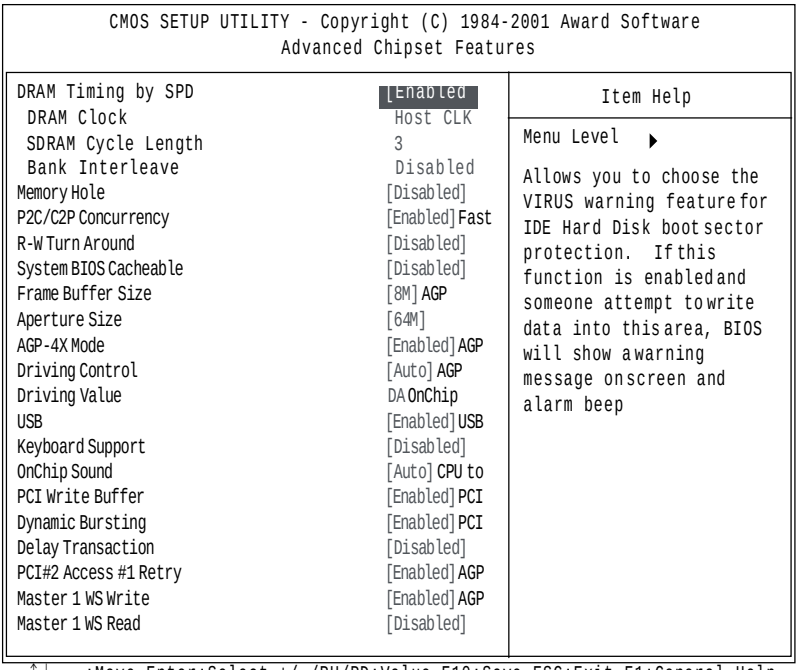
OS Select For DRAM > 64MB
Select the operating system that is running with greater than 64MB of RAM on the system.The choice: Non-OS2, OS2.

Video BIOS Shadow
Enabled this copies the video BIOS from ROM to RAM. effectively enhancing performance, and reducing the amount of upper memory available by 32KB (the C0000~C7FFF area of memory between 640 KB and 1 MB is used).

C8000-CBFFF Shadow
Enabling any of the C8000~CBFFF segments allows components to move their firmware into these upper memory segments. However your computer can lock-up doing so, because some devices don't like being shadowed at those particular 16 KB segments of upper memory.

Note - In Windows 95, double click 'Computer' within Device Manager and select 'Memory'. This will tell you what segments (if any) are being shadowed For DOS you can use MSD.EXE to see what segments are claimed.
CC000-CFFFF - D0000-D3FFF - D4000-D7FFF - D8000-DBFFF and DC000-DFFFF - Same as above.

Chipset Features Setup



DRAM Timing By SPD

If your DIMM memory have SPD (Serial Presence Detect) 8-pin IC on module, you can set this option to Enabled. System will set your DRAM clock and timing from the SPD IC. If the option set as Disabled, DRAM clock and timing must be set from items below. (DRAM Clock, SDRAM Cycle Length and Bank Interleave)

DRAM Clock

This item allows you to set the DRAM Clock. Options are Host CLK, HCLK+33M or HCLK-33M. Please set the item according to the Host (CPU) Clock and DRAM Clock.

SDRAM Cycle Length

This feature is similar to SDRAM CAS Latency Time. It controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. Thus, the lower the cycle length, the faster the transaction. However, some SDRAM cannot handle the lower cycle length and may become unstable. So, set the SDRAM Cycle Length to 2 for optimal performance if possible but increase it to 3 if your system becomes unstable.

Bank Interleave
This feature enables you to set the interleave mode of the SDRAM interface. Interleaving allows banks of SDRAM to alternate their refresh and access cycles. One bank will undergo its refresh cycle while another is being accessed. This improves performance of the SDRAM by masking the refresh time of each bank. A closer examination of interleaving will reveal that since the refresh cycles of all the SDRAM banks are staggered, this produces a kind of pipelining effect. If there are 4 banks in the system, the CPU can ideally send one data request to each of the SDRAM banks in consecutive clock cycles. This means in the first clock cycle, the CPU will send an address to Bank 0 and then send the next address to Bank 1 in the second clock cycle before sending the third and fourth addresses to Banks 2 and 3 in the third and fourth clock cycles respectively. Each SDRAM DIMM consists of either 2 banks or 4 banks. 2-bank SDRAM DIMMs use 16Mbit SDRAM chips and are usually 32MB or less in size. 4-bank SDRAM DIMMs, on the other hand, usually use 64Mbit SDRAM chips though the SDRAM density may be up to 256Mbit per chip. All SDRAM DIMMs of at least 64MB in size or greater are 4-banked in nature.

If you are using a single 2-bank SDRAM DIMM, set this feature to 2-Bank. But if you are using two 2-bank SDRAM DIMMs, you can use the 4-Bank option as well. With 4-bank SDRAM DIMMs, you can use either interleave options. Naturally, 4-bank interleave is better than 2-bank interleave so if possible, set it to 4-Bank. Use 2-Bank only if you are using a single 2-bank SDRAM DIMM. Notethat it is recommends that SDRAM bank interleaving be disabled if 16Mbit SDRAM DIMMs are used.

Memory Hole
Enabling this feature reserves 15MB to 16MB memory address space to ISA expansion cards that specifically require this setting. This makes the memory from 15MB and up unavailable to the system. Expansion cards can only access memory up to 16MB.

P2C/C2P Concurrency
When Disabled, CPU bus will be occupied during the entire PCI operation period.

Fast R-W Turn Around
This BIOS option reduces the delay that occurs when the CPU first reads from the RAM and then writes to it. There is normally an extra delay associated with this switch from reading to writing. If you enable this option, the delay will be reduced and switching from read to write will be faster. However, if your RAM modules cannot handle the faster turnaround, data may be lost and your system may become unstable. With that in mind, enable this option for better RAM performance unless you face stability problems after enabling it.

System BIOS Cacheable
Allows the system BIOS to be cached for faster system performance.

Frame Buffer Size
This item defines the amount of system memory that will be shared and uses

AGP Aperture Size
Options : 4, 8, 16, 32, 64, 128, 256

This option selects the size of the AGP aperture. The aperture is a portion of the PCI memory address range dedicated as graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without need for translation. This size also determines the maximum amount of system RAM that can be allocated to the graphics card for texture storage.

AGP Aperture size is set by the formula : maximum usable AGP memory size x 2 plus 12MB. That means that usable AGP memory size is less than half of the AGP aperture size. That's because the system needs AGP memory (uncached) plus an equal amount of write combined memory area and an additional 12MB for virtual addressing. This is address space, not physical memory used. The physical memory is allocated and released as needed only when Direct3D makes a "create non-local surface" call.

AGP-4X Mode
Set to Enabled if your AGP card supports the 4X mode, which transfers video data at 1066MB/s.

AGP Driving Control
This item is use for control AGP drive strength.
Auto: Setup AGP drive strength by default setting.
Manual: Setup AGP drive strength by manual setting.

AGP Driving Value
Key in a HEX number to control AGP output buffer drive strength.
Min = 00, Max = FF.

OnChip USB
If your system contains a Universal Serial Bus controller and you have a USB peripheral, select Enabled. The next option will become available.

USB Keyboard Support
This item lets you enable or disable the USB keyboard driver within the onboard BIOS.

CPU to PCI Write Buffer
This controls the CPU write buffer to the PCI bus. If this buffer is disabled, the CPU writes directly to the PCI bus. Although this may seem like the faster and thus, the better method, this isn't true. Because the CPU bus is faster than the PCI bus, any CPU writes to the PCI bus has to wait until the PCI bus is ready to receive data. This prevents the CPU from doing anything else until it has completed sending the data to the PCI bus. Enabling the buffer enables the CPU to immediately write up to 4 words of data to the buffer so that it can continue on another task without waiting for those 4 words of data to reach the PCI bus. The data in the write buffer will be written to the PCI bus when the next PCI bus read cycle starts. The difference here is that it does so without stalling the CPU for the entire CPU to PCI transaction. Therefore, it's recommended that you enable the CPU to PCI write buffer.

PCI Dynamic Bursting
When enabled, data transfer on the PCI bus, where possible, make use of the high-performance PCI bust protocol, in which greater amounts of data are transferred at a single command.

PCI Master 0 WS Write
This function determines whether there's a delay before any writes to the PCI bus. If this is enabled, then writes to the PCI bus are executed immediately (with zero wait states), as soon as the PCI bus is ready to receive data. But if it is disabled, then every write transaction to the PCI bus is delayed by one wait state. Normally, it's recommended that you enable this for faster PCI performance. However, disabling it may be useful when overclocking the PCI bus results in instability. The delay will generally improve the overclockability of the PCI bus.

PCI Delay Transaction
The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.

PCI # 2 Access # 1 Retry
This BIOS feature is linked to the CPU to PCI Write Buffer. Normally, the CPU to PCI Write Buffer is enabled. All writes to the PCI bus are, as such, immediately written into the buffer, instead of the PCI bus. This frees up the CPU from waiting till the PCI bus is free. The data are then written to the PCI bus when the next PCI bus cycle starts.

There's a possibility that the buffer write to the PCI bus may fail. When that happens, this BIOS option determines if the buffer write should be reattempted or sent back for arbitration. If this BIOS option is enabled, then the buffer will attempt to write to the PCI bus until successful. If disabled, the buffer will flush its contents and register the transaction as failed. The CPU will have to write again to the write buffer. It is recommended that you enable this feature unless you have many slow PCI devices in your system. In that case, disabling this feature will prevent the generation of too many retries which may severely tax the PCI bus.

AGP Master 1 WS Write
By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a write transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP write performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

AGP Master 1 WS Read
By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a read transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP read performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

Integrated Peripherals

```
CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software
Integrated Peripherals

OnChip IDE Channel0          [Enabled]
OnChip IDE Channel1          [Enabled]
IDE Prefetch Mode            [Enabled]
Primary Master PIO           [Auto] Primary
Slave PIO                    [Auto]
Secondary Master PIO         [Auto]
Secondary Slave PIO          [Auto] Primary
Master UDMA                  [Auto] Primary
Slave UDMA                   [Auto]
Secondary Master UDMA        [Auto]
Secondary Slave UDMA         [Auto] Init
Display First                [PCI Slot] IDE
HDD Block Mode               [Enabled]
Onboard FDD Controller       [Enabled]
Onboard Serial Port 1        [Auto] Onboard
Serial Port 2                [Auto] UART 2
Mode                         [Standard] IR
Function Duplex              Half Tx, Rx
inverting enable             No, Yes
Onboard Parallel Port        [378/IRQ7]
Onboard Parallel Mode        [Normal] ECP
Mode Use DMA                 3
Parallel Port EPP Type       EPP1.9
Onboard Legacy Audio         [Enabled]
Sound Blaster                [Disabled]
SB I/O Base Address          [220H] SB IRQ
Select                       [IRQ 5] SB
DMA Select                   [DMA1]
MPU-401                      [Disabled]
MPU-401 I/O Address          [330-333H]

Item Help

Menu Level ▶

Allows you to choose the VIRUS warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F6:Fail-SAfe Defaults F7:Optimized Defaults
```

OnChip IDE Channel 0/1
Select "Enabled" to activate each on-board IDE channel separately, Select "Disabled", if you install an add-on IDE Control card

IDE Prefetch Mode
Enable prefetching for IDE drive interfaces that support its faster drive accesses. If you are getting disk drive errors, change the setting to omit the drive interface where the errors occur. Depending on the configuration of your IDE subsystem, this field may not appear, and it does appear when the Internal PCI/IDE filed, above, is Disabled.

Primary & Secondary Master/Slave PIO
These four PIO fields let you set a PIO mode (0-4) for each of four IDE devices. When under "Auto" mode, the system automatically set the best mode for each device

Primary & Secondary Master/Slave UDMA
When set to "Auto" mode, the system will detect if the hard drive supports Ultra DMA mode.

Init Display First
Select "AGP" or "PCI Slot" for system to detect first when boot-up.

IDE HDD Block Mode
This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

Onboard FDD Controller
Select "Enabled" to activate the on-board FDD
Select "Disabled" to activate an add-on FDD

Onboard Serial Port 1 & 2
Select an address and corresponding interrupt for the first/second serial port. The default value for the first serial port is "3F8/IRQ4" and the second serial port is "2F8/IRQ3".

UART 2 Mode
Select to activate the Infrared transfer function.

Onboard Parallel Port
Select address and interrupt for the Parallel port.

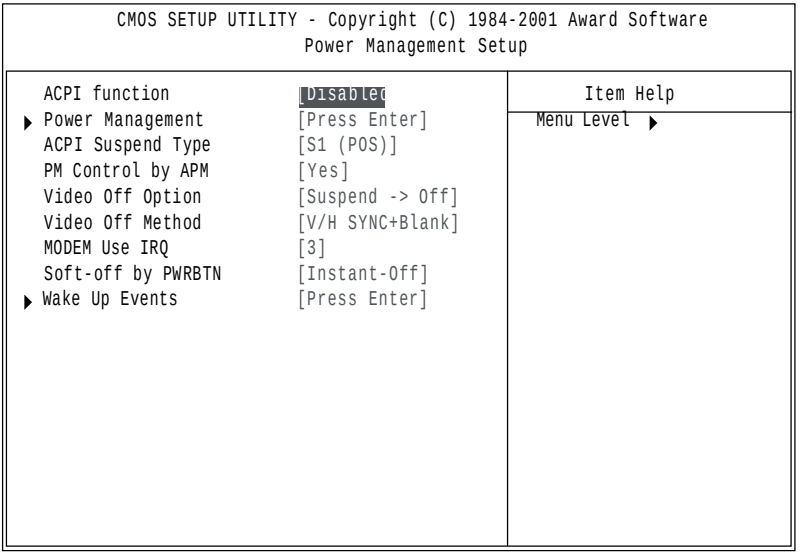
Onboard Parallel Mode
Select an operating mode for the parallel port. Mode options are Normal, EPP, ECP, ECP/EPP.

ECP Mode Use DMA
Select a DMA channel if parallel Mode is set as ECP, ECP/EPP.

Parallel Port EPP Type
Select a EPP Type if parallel Port is set as EPP, ECP/EPP.

Onboard Legacy Audio
Configuration options: Enabled and Disabled. When Enabled, select additional settings for SoundBlaster Compatibillity and MPU-401 functionallity

Power Management Setup



ACPI Function
Select Enabled only if your computer's operating system supports ACPI (the Advanced Configuration and Power Interface) specification. Currently, Windows 98 and Windows2000 support ACPI.

Power Management
There are 4 selections for Power Management, 3 of which have fixed mode :

Disabled (default)	No power management. Disables all four modes.
Min. Power Saving	Minimum power management. Doze Mode = 1 hr., Standby Mode = 1 hr., Suspend Mode = 1 hr.,
Max. Power Saving	Maximum power management -- ONLY AVAILABLE FOR SL CPU's.. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min.
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr.

HDD Power Down is always set independently

ACPI Suspend Type
S1 (POS) Power On suspend
All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive and PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthe- sizer. The only power consumed in the system is due to DRAM Refresh and leakage current of the powered devices. When the system resumes from POS, PIIX4 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, PIIX4 only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

S3 (STR) Suspend To RAM
Power is removed from most of the system components during STR, except the DRAM. Power is supplied to Suspend Refresh logic in the Host Controller, and RTC and Suspend Well logic in PIIX4. PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

PM Control By APM
When enabled, an Advanced power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock. If the Max. Power Saving is not enabled, this will be preset to No.

Video Off Option
Controls what causes the display to be switched off
Suspend -> Off Always On All Mode -> Off

Video Off Method
This determines the manner in which the monitor is blanked.

V/H SYNC+Blank	cause the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.
Blank Screen	This option only writes blanks to the screen.
DPMS	Initial display power management signaling.

Modem Use IRQ
Name the interrupt request (IRQ) assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.

Soft-Off By PWRBTN
The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means powering off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is pressed for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when press for less than four seconds. The default is 'Instant-Off'.

Wake Up Events

Setting an event on each device listed to awaken the system from a soft off state.

VGA

LPT & COM

HDD & FDD

PCI Master

Power On by PCI Card

Wake Up on LAN/Ring

RTC Alarm Resume

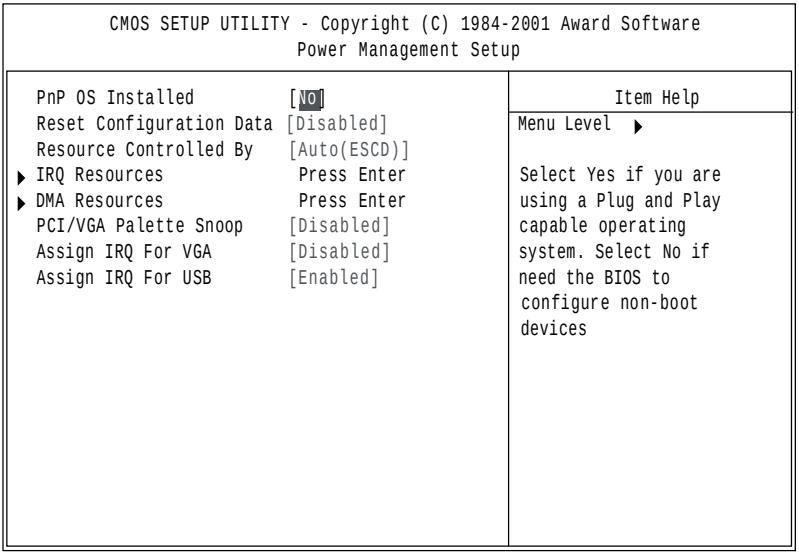
Date (of Month)

Resume Time (hh:mm:ss)

Primary INTR

IRQs Activity Monitoring

PnP/PCI Configuration



This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

PnP OS Installed

Select Yes if the system operating environment is Plug-and-Play aware (e.g., Windows 95).

Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset ESCD (Extended System Configuration Date) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

Resource Controlled By

The Award Play and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

IRQ Resources
When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt :

Legacy ISA Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP Device compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

DMA Resources
When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the DMA :

Legacy ISA Devices compliant with the original PC/AT bus specification, requiring a specific DMA channel.

PCI/ISA PnP Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

PCI/VGA Palette Snoop
Normally this option is always Disabled! Nonstandard VGA display adapters such as overlay cards or MPEG video cards may not show colors properly. Setting Enabled should correct this problem. If this field set Enabled, any I/O access on the ISA bus to the VGA card's palette registers will be reflected on the PCI bus. This will allow overlay cards to adapt to the changing palette colors.

Assign IRQ For VGA
Many high-end graphics accelerator cards now require an IRQ to function properly. Disabling this feature with such cards will cause improper operation and/or poor performance. Thus, it's best to make sure you enable this feature if you are having problems with your graphics accelerator card. However, some low-end cards don't need an IRQ to run normally. Check your graphics card's documentation (manual). If it states that the card does not require an IRQ, then you can disable this feature to release an IRQ for other uses. When in doubt, it's best to leave it enabled unless you really need the IRQ.

Assign IRQ For USB
Windows 95 will automatically give an IRQ to the USB port even if there is no USB peripheral connected. Disabling this will free the IRQ.

POST Codes

The following codes are not displayed on the screen. They can only be viewed on the LED display of a so called POST card. The codes are listened in the same order as the according functions are executed at PC startup. If you have access to a POST Card reader, you can watch the system perform each test by the value that's displayed. If the system hangs (if there's a problem) the last value displayed will give you a good idea where and what went wrong, or what's bad on the system board.

CODE	DESCRIPTION OF CHECK
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved

0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial onboard clock generator if Early_Init_Onboard_Generator is defined. See also POST 26h.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead.
24h	Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.

25h	Early PCI Initialization: -Enumerate PCI bus number. -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0
26h	1. If Early_Init_Onboard_Generator is not defined Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 2. Init onboard PWM 3. Init onboard H/W monitor devices
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed.
2Ah	Reserved
2Bh	Invoke Video BIOS
2Ch	Reserved
2Dh	1. Initialize double-byte language font (Optional) 2. Put information on screen display, including Award title, CPU type, CPU speed, full screen logo.
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977 series Super I/O chips. See also POST 63h.
34h	Reserved
35h	Test DMA Channel 0
36h	Reserved
37h	Test DMA Channel 1.
38h	Reserved
39h	Test DMA page registers.
3Ah	Reserved
3Bh	Reserved

3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	1. Calculate total memory by testing the last double word of each 64K page. 2. Program write allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	1. Program MTRR of M1 CPU 2. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range. 3. Initialize the APIC for P6 class CPU. 4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB Keyboard & Mouse.
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Clear password according to H/W jumper (Optional)
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved

57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO 2. Initialize Init_Onbaord_AUDIO.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reset keyboard if Early_Reset_KB is not defined.
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved

71h	Reserved
72h	Reserved
73h	(Reserved
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	(Optional Feature) Enter AWDFLASH.EXE if: -AWDFLASH.EXE is found in floppy drive. -ALT+F2 is pressed.
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Init HDD write protect.
7Dh	Reserved
7Eh	Reserved
7Fh	Switch back to text mode if full screen logo is supported. - If errors occur, report errors & wait for keys - If no errors occur or F1 key is pressed to continue : wClear EPA or customization logo.
80h	Reserved
81h	Reserved

E8POST.ASM starts

82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. Switch screen back to text mode
86h	Reserved
87h	NET PC: Build SYSID Structure.
88h	Reserved

89h	1. Assign IRQs to PCI devices 2. Set up ACPI table at top of the memory.
8Ah	Reserved
8Bh	1. Invoke all ISA adapter ROMs 2. Invoke all PCI ROMs (except VGA)
8Ch	Reserved
8Dh	1. Enable/Disable Parity Check according to CMOS setup 2. APM Initialization
8Eh	Reserved
8Fh	Clear noise of IRQs
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	1. Enable L2 cache 2. Program Daylight Saving 3. Program boot up speed 4. Chipset final initialization. 5. Power management final initialization 6. Clear screen & display summary table 7. Program K6 write allocation 8. Program P6 class write combining
95h	Update keyboard LED & typematic rate
96h	1. Build MP table 2. Build & update ESCD 3. Set CMOS century to 20h or 19h 4. Load CMOS time into DOS timer tick 5. Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)

Howto : Flash the BIOS

To flash your BIOS you'll need

1) a xxxxx.bin file that is a file image of the new BIOS

2) AWDFLASH.EXE a utility that can write the data-file into the BIOS chip.

Create a new, clean DOS 6 bootable floppy with "format a: /s".

Copy flash utility and the BIOS image file to this disk.

Turn your computer off. Insert the floppy you just created and boot the computer. As it boots up, hit the [DEL] key to enter the CMOS setup. Go to "LOAD SETUP (or BIOS) DEFAULTS," and then save and exit the setup program. Continue to boot with the floppy disk.

Type "AWDFLASH" to execute the flash utility. When prompted, enter the name of the new BIOS image and begin the flash procedure. Note: If you reboot now, you may not be able to boot again.

After the flash utility is complete, reboot the system.

What to do when the Award flasher says: Insufficient memory

1. In CMOS Chipset Features Setup, Disable Video Bios Cacheable.

2. Hit Esc, F10, Save and exit.

3. Flash the BIOS and reboot

4. Enter CMOS Chipset Features Setup,and Enable Video Bios Cacheable, hit Esc, F10, Save and reboot.

What if things go wrong

if you use the wrong Flash BIOS or if the writing process gets interrupted, there is a fat chance that your computer won't boot anymore.

How can you recover a corrupt BIOS ?

Boot-block booting (this works only for Award BIOS)

Modern motherboards based on Award BIOS have a boot-block BIOS. This is small area of the BIOS that doesn't get overwritten when you flash a BIOS. The boot-block BIOS only has support for the floppy drive. If you have the AGP video enabled you won't see anything on the screen because the boot-block BIOS only supports an ISA videocard.

If you do not want to change your AGP video setting than proceed as follows:

The boot-block BIOS will execute an AUTOEXEC.BAT file on a bootable diskette. Copy an Award flasher & the correct BIOS *.bin file on the floppy and execute it automatically by putting awdflash *.bin in the AUTOEXEC.BAT file.

Solution 2: Hot-swapping

1. Replace the corrupt chip by a working one. The working BIOS doesn't have to be written for your board, it just has to give you a chance of booting to DOS.

BIOSs for the same chipset mostly work. (Chipsets that not differ too much also mostly work. (e.g. Triton FX chipset and Triton HX chipset)

2. Boot the system to DOS (with floppy or HD)

3. Be sure that the System BIOS cacheable option in your BIOS is enabled! If so replace (while the computer is powered on) the BIOS chip with the corrupt one. This should work fine with most boards because the BIOS is shadowed in RAM.

4. Flash an appropriate BIOS to the corrupt chip and reboot.

NOTE: Use a flasher from MRBIOS (http://www.mrbios.com). Utilities that come with your motherboard often use specific BIOS-hooks. Because you have booted with a BIOS not written for your motherboard they usually don't work. The MR Flash utilities communicate directly with your Flash Rom and always work. In most cases they flash a non-MRBIOS to your BIOS chip without problems.

Contact Information

Thank you for purchasing from Global American Inc. We will stand by our slogan,

Integration with Integrity.

Please let us know how your product is performing and if we can help you with any
future product lines.

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