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User's Manual

Single Board Computer 3307760

Version 1.0, 2007

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your 3307760 system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory to get a safe installation and provides a programming guide of Watch Dog Timer function.

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Chapter 1
System Overview

1.1 Introduction

PICMG organization published the PICMG 1.3 specification in late year 2005 which adopts PCI Express as external I/O expansion interface. The advanced PCI Express Technology's throughput balanced the modern extreme computing power that makes the system much more powerful.

3307760, the PICMG 1.3 SHB (Single Host Board) supports the Intel® Core 2 Duo processor that are based on Intel® innovated Core Microarchitecture. The attractive processor does not only posses amazing parallel computing power but also generates 65W TDP (Thermal Design Power). That makes the system more powerful and reliable with dual-core processors with a smaller and quieter cooling fan.

The SHB was empowered by Intel® Q965 & ICH8DO chipset. The Q965 embedded Graphics Media Adapter 3000 is the 4th generation Intel integrated graphics controller that supports DirectX 9.0, Shader model 2.0, 256MB of video memory. More than that, user could utilize even higher-end, the latest PCI Express x16 interface graphics card via backplane.

To meet bandwidth of storage and expansion cards requirements, the 3307760 was designed to be flexible with four PCI Express lanes via backplane. Those four PCI Express lanes could be four PCI Express x1 links or one PCI Express x4 link. A four PCI Express x1 link configuration can support more PCI Express x1 devices via backplane and one PCI Express x4 link configuration can support a RAID card or special add-on cards such as an image processing board. In addition, the flexible configuration can be leveraged with a bridge backplane to support more PCI or PCI-X slots that benefits industries with legacy support.

Advanced Management Technology (AMT) is a feature that the 3307760 comes equipped with. This technology provides remote access capability via the Intel® Gigabit Ethernet controller. With software from a 3rd party, the new technology allows MIS or users to monitor system status and help the client to recover from a system failure. Besides that, the hardware and software information can be gathered by 3rd party software and then stored in SPI interface EEPROM. Therefore, asset management could be done at the same time.

3307760 features:

- Support Intel® Core 2 Quad, Intel® Core 2 Duo, Pentium® D, Pentium® 4, Celeron® D processor in an LGA775 socket equipped with dual core, Hyper-Threading, EM64T, EIST, XD & VT technologies
- Dual 240-pin DDR2 SDRAM DIMM sockets, support for DDR2 800/667/533 DIMMs, up to 4GB system memory
- Intel® Q965 integrated GMA 3000 on-board graphics delivers richer visual color and picture clarity
- Equipped dual Gigabit Ethernet ports
- One PCI Express x16 external expansion fulfills visual
- Configurable four external PCI Express lanes (one x4 or four x1)

The PICMG 1.3 SHB is the best solution of applications like flight simulation, image processing, broadcasting and so on that need performance of display and storage.

1.2 Check List

The 3307760 package should cover the following basic items:

- ✓ One 3307760 single host board
- ✓ One dual Serial ports cable kit
- ✓ One single Parallel port cable kit
- ✓ One FDD cable
- ✓ Two 7-pin SATA signal cables
- ✓ One Installation Resources CD-Title
- ✓ One booklet of 3307760

Optional: One bracket with PS/2 keyboard and mouse

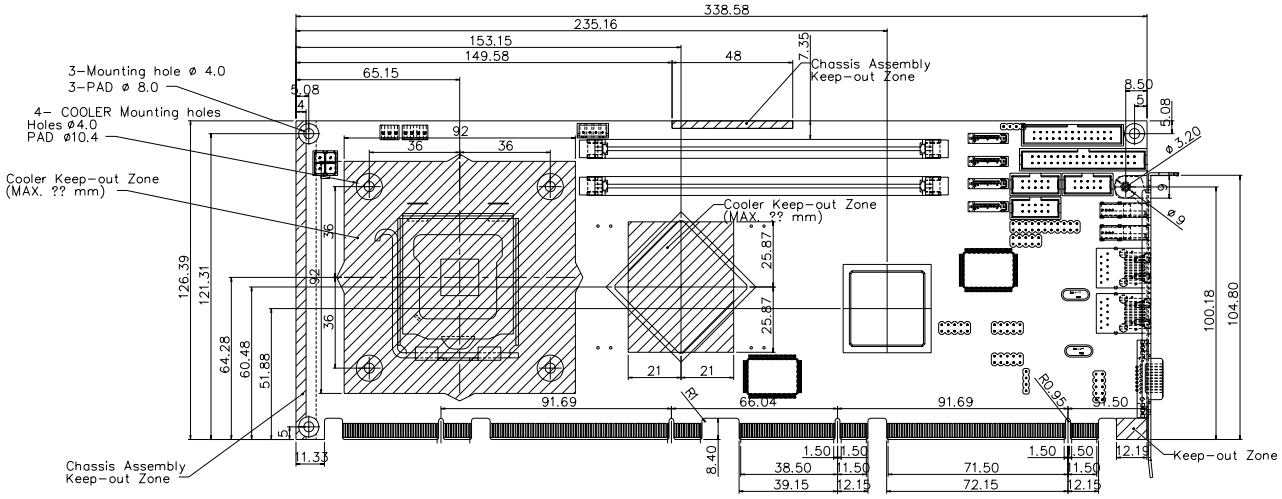
If any of these items are damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

Table of Contents

How to Use This Manual

- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention
- **Watchdog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - Generate system reset
- **On-board VGA**
  GMCH integrated graphics, 400MHz core frequency; share system memory up to 64MB for system with greater than or equal to 192MB of system memory
- **On-board Ethernet LAN**
  Dual Intel® PCI Express x1 interface based Gigabit Ethernet to support RJ-45 connector
- **High Driving GPIO**
  Support 8 programmable high driving GPIO
- **Cooling Fans**
  Support one 4-pin power connector for CPU fan and one 3-pin power connector for system fan
- **System Monitoring Feature**
  Monitor CPU temperature, system temperature and major power sources, etc.
- **Bracket**
  Support dual Ethernet port with 2 indicators, dual USB ports and one CRT port
- **Outline Dimension (L X W):**
  338.5mm (13.33") X 122mm (4.8")
- **Power Requirements:**
  - +12V@ 3.4A
  - +5V @ 4.5A
  - Test configuration:
    - CPU: Intel® Core 2 Duo 2.13GHz(FSB: 1,066 / L2 cache: 2MB)
    - Memory: Transcend (SAMSUNG-K4T51083QC-ZCE7) 512GBx2 DDRII 800
    - Primary Master SATA HDD: HITACHI-HDS721680PLA380 (82GB)
    - OS: Microsoft Windows XP Professional + SP2
    - Test Programs: Burning Test V5.0
    - Run Time: Full loading
- **Operating Temperature:**
  0°C ~ 60°C (23°F ~ 140°F)
- **Storage Temperature:**
  -20°C ~ 80°C
- **Relative Humidity:**
  5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



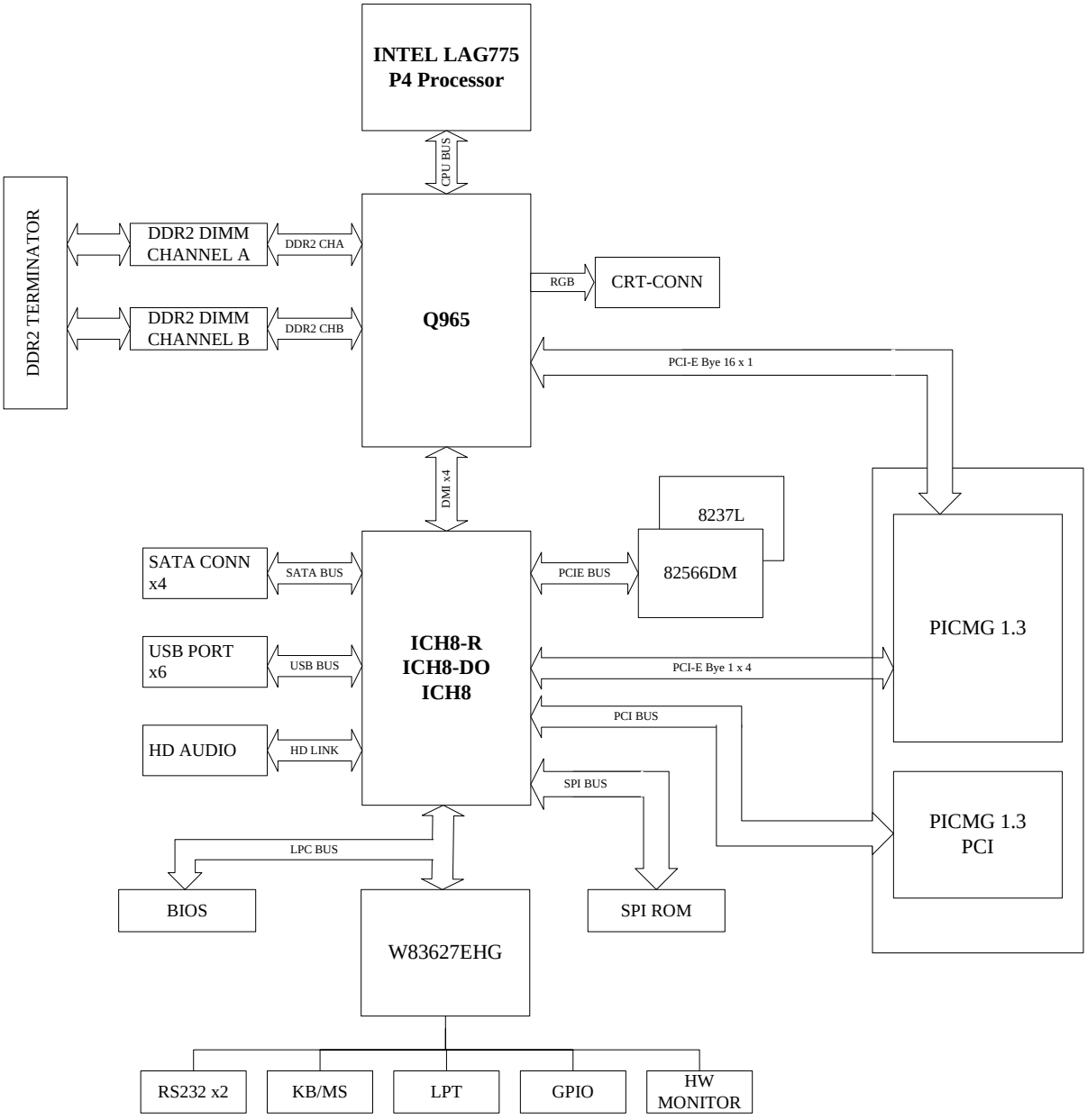
1.4 System Architecture

3307760 adopts Intel® Q965 Express chipset that supports Intel® Core 2 Duo processor that based on Intel innovative Core Mircoarchitecture Technology. Q965 GMCH (Graphics Memory Controller Hub) embedded Graphics Media Accelerator 3000 (GMA 3000) and features PCI Express x16 graphics interface via backplane that supports the latest high-performance graphics cards. Along with the highest 1,066MHz FSB of processor, the parallel system memory up to DDR2 800 as well.

The companion I/O controller, ICH8DO has six PCI Express x1 links that throughput is 2.5Gbps per direction. And they were designed as interface of dual Gigabit Ethernet ports on-board and four PCI Express x1 expansion via backplane. One special characteristic of the ICH8DO is the capability to aggregate these four PCI Express x1 link as on PCI Express x4 link. And that is what user can benefit for PCI Express x4, high throughput storage expansion card via backplane.

ICH8DO provides six SATA 300 ports, together with Intel® Matrix Storage Technology (MST), the 3307760 offers cost effective RAID 0, 1, 5 and 10 that seamlessly protects against data loss from hard drive failure. Dual SATA ports and dual USB ports are routed to gold finger for better wiring consideration of these two kinds of interface via backplane.

Super I/O chip, W83627 is responsible for PS/2 keyboard/mouse, UARTs, FDC, hardware monitor, Parallel, and Watch Dog Timer interface.



3307760 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connector. All of the configuration jumpers on 3307760 series are in the proper position. The default settings shipped from factory are marked with a star (★).

2.1 Jumper Setting

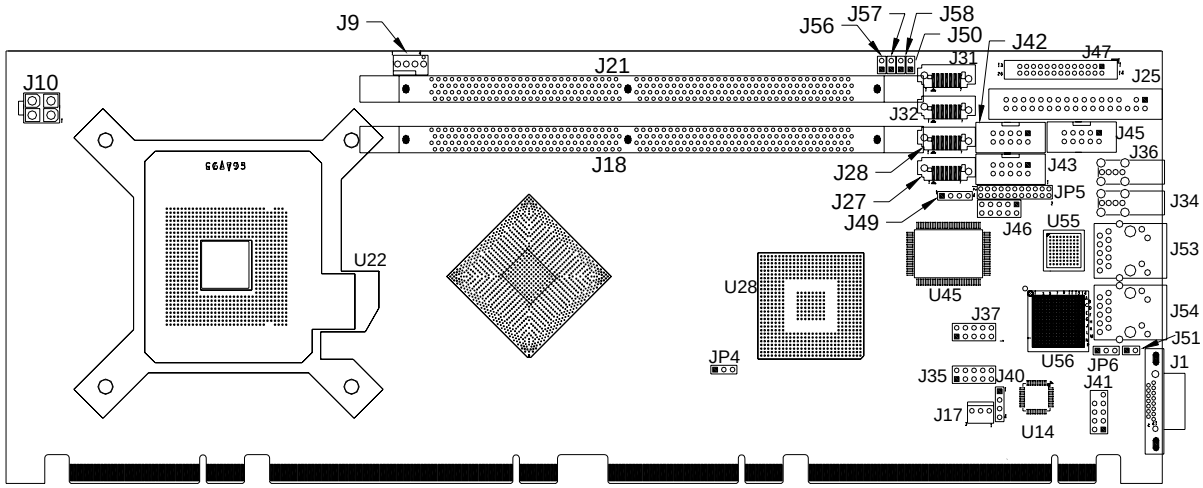


Figure 2-1 3307760 Jumper Location

JP4: CMOS Clear

JP4	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents

JP5: COM2 (J43) Interface Selection

JP5	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

JP6: Intel 82573L Interface Selection

Reserve for Enable or disable LAN function.
Normal control at 1-2 short.

J56/J57: PCI-E X1,X4 Interface Selection

J56,J57	Function
Short	PCI-E X4 (Support one slot)
Open	PCI-E X1 (Support four slot) ★

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors on this Single Board Computer.

Connector Function List

Connector	Description	Remark
J1	VGA D-SUB Connector	
J9	FAN 1 (CPU FAN) Power Connector	
J10	+12V Power Connector	
J17	FAN 2 (SYSTEN FAN) Power Connector	
J18	DDR2 SDRAM SLOT	
J21	DDR2 SDRAM SLOT	
J25	Floppy Connector	
J27	SATA 3 Connector	
J28	SATA 2 Connector	
J31	SATA 0 Connector	
J32	SATA 1 Connector	
J34	External USB Connector	
J35	Internal USB Connector	
J36	External USB Connector	
J37	Internal USB Connector	
J40	Audio CD -IN Connector	
J41	Audio Connector	
J42	COM1 Serial Port 1 Connector	
J43	COM2 Serial Port 2 Connector	
J45	External PS/2 Keyboard/Mouse Connector	
J46	General Purpose I/O Connector	
J47	Parallel Port Connector	
J49	External Speaker Connector	

J50	Suspend LED	
J51	SATA LED	
J53	Ethernet RJ-45 Connector (LAN 1)	
J54	Ethernet RJ-45 Connector (LAN 2)	
J55	Reserve	
J58	Power LED	

Pin Assignments of Connectors

J1: On-board VGA Connector

PIN No.	Signal Description
1	Red
2	Green
3	Blue
4	Monitor ID0 (MONID0) (5V I/F)
5	Ground
6	Ground
7	Ground
8	Ground
9	+5V
10	Ground
11	Monitor ID1 (MONID1) (5V I/F)
12	VGA DDC Data (5V I/F)
13	Horizontal Sync. (HSYNC) (5V I/F)
14	Vertical Sync. (VSYNC) (5V I/F)
15	VGA DDC Clock (5V I/F)

J9: CPU Fan Connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Control
4	Fan Speed Detecting signal

J10: +12V POWER Connector

PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

J17: System Fan Connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Speed Detecting signal

J25: FDC Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select 0
3	Ground	4	N/C
5	Ground	6	Density Select 1
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor ENB#
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Head Select#
33	Ground	34	Disk Change#

J31/J32/J28/J27: Primary/Secondary/3rd/4th SATA Connector

PIN No.	Signal Description
1	Ground
2	SATATX+ (SATATXP)
3	SATATX- (SATATXN)
4	Ground
5	SATARX- (SATARXN)
6	SATARX+ (SATARXP)
7	Ground

J34/J36: External USB Connector

PIN No.	Signal Description
1	5V Dual
2	USB0-
3	USB0+
4	Ground

J35/J37: Internal USB Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	5V Dual
3	Ground	4	USB3-
5	USB2+	6	USB3+
7	USB2-	8	Ground
9	5V Dual	10	Ground

Note:
5V Dual is always available. It's supplied by either 5V VCC power source in normal operation mode or 5V standby power source in standby mode.

J40: Audio CD-IN Connector

PIN No.	Signal Description
1	CD-in Left Channel
2	CD Ground
3	CD Ground
4	CD-in Right Channel

J41: Audio MIC/Line-in/Line-out Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	MIC with Reference Voltage	2	Analog Ground
3	Line-in Left Channel	4	Analog Ground
5	Line-in Right Channel	6	Analog Ground
7	Line-out Left Channel	8	Analog Ground
9	Line-out Right Channel	10	N/C

J42: COM1 Serial Port 1 Connector

PIN No.	Signal Description
1	DCD (Data Carrier Detect)
2	RXD (Receive Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	GND (Ground)
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)
10	N/C

J43 : COM2 Serial Port 2 Connector

PIN No.	Signal Description		
	RS-232	**RS-422**	**RS-485**
1	DCD (Data Carrier Detect)	TX-	DATA-
2	RXD (Receive Data)	TX+	DATA+
3	TXD (Transmit Data)	RX+	N/C
4	DTR (Data Terminal Ready)	RX-	N/C
5	GND (Ground)	GND	GND
6	DSR (Data Set Ready)	N/C	N/C
7	RTS (Request to Send)	N/C	N/C
8	CTS (Clear to Send)	N/C	N/C
9	RI (Ring Indicator)	N/C	N/C
10	N/C	N/C	N/C

Note:
J43 (COM2) could be configurable as RS-232/422/485 with jumper JP5.

J45: External PS/2 Keyboard/Mouse Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Mouse Clock

J46: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

Note:
All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each Fan.

J47: Parallel Port Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	14	Auto Form Feed#
2	Data 0	15	Error#
3	Data 1	16	Initialization#
4	Data 2	17	Printer Select IN#
5	Data 3	18	Ground
6	Data 4	19	Ground
7	Data 5	20	Ground
8	Data 6	21	Ground
9	Data 7	22	Ground
10	Acknowledge#	23	Ground
11	Busy	24	Ground
12	Paper Empty	25	Ground
13	Printer Select	26	N/C

J49: External Speaker Connector

PIN No.	Signal Description
1	Speaker Signal Output (Open-drain w/ internal series 33 Ohm)
2	N/C
3	Ground
4	+5V

Note:
The pull-high voltage of external speaker is limited at 5V maximum.

J50: Suspend LED Connector

PIN No.	Signal Description
1	Ground
2	5V_DUAL

J51: Suspend LED Connector

PIN No.	Signal Description
1	SATA LED Signal
2	3.3V

J53/J54 : Ethernet RJ-45 Connector

PIN No.	Signal Description
1	MDI0+ (MDI0P)
2	MDI0- (MDI0N)
3	MDI1+ (MDI1P)
4	MDI2+ (MDI2P)
5	MDI2- (MDI2N)
6	MDI1- (MDI1N)
7	MDI3+ (MDI3P)
8	MDI3- (MDI3N)

J58: Power LED Connector

PIN No.	Signal Description
1	Ground
2	3.3V

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you handle WDT and GPIO operation in software programming.

3.1 Intel® LGA775 Processor

Installing LGA775 CPU

1) Lift the handling lever of CPU socket outwards and upwards to the other end. Following step A position to step B position.

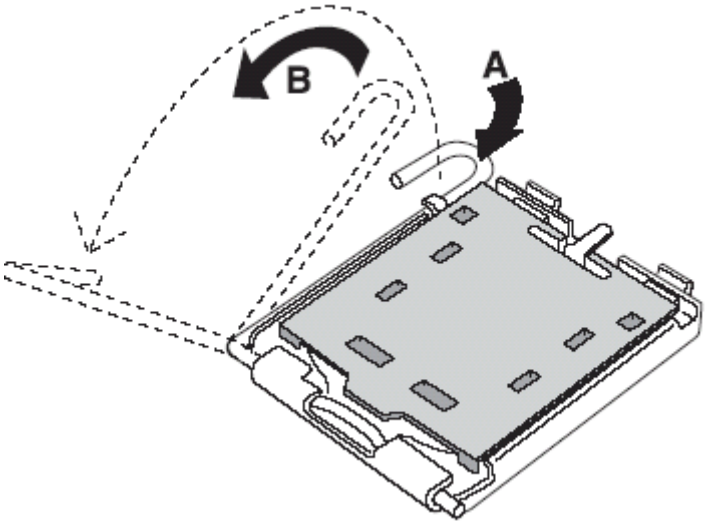


Figure 3-1

2) Aligning the processor's pins with pinholes on the socket, and then make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into correct place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.

Triangle mark is meaning first pin position; kindly assemble and take aim at notch of top and bottom between CPU and socket.

Figure 3-2

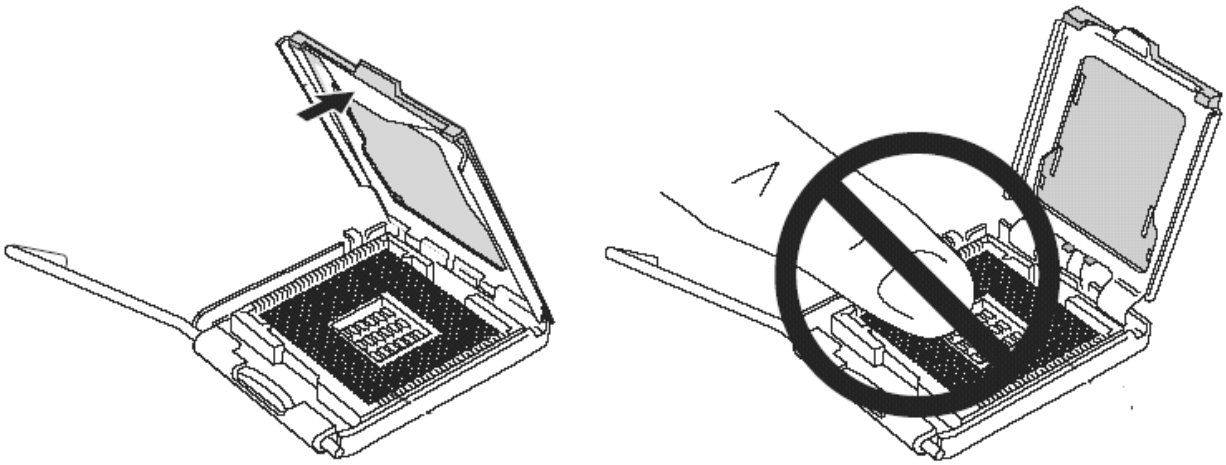


Figure 3-3

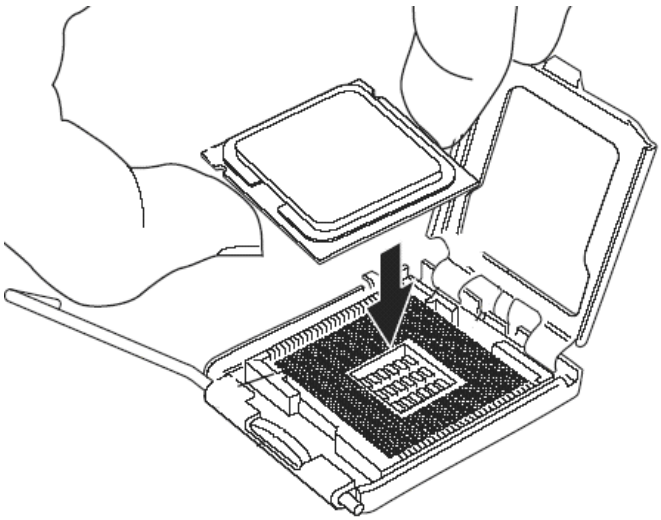


Figure 3-4

Precaution! (See fig.3-3 and fig.3-4) Don't touch directly by your hand or impacts internal align balls of CPU socket to avoid motherboard destruction, it is a precise actuator.

3) Push down the lever to lock processor chip into the socket once CPU fits.

4) Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the LGA775.

Removing CPU

1) Unlock the cooling fan first.
2) Lift the lever of CPU socket outwards and upwards to the other end.
3) Carefully lifts up the existing CPU to remove it from the socket.
4) Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

Configuring System Bus

3307760 will automatically detect the CPU used. All of CPU speed of Intel® Pentium® D, Pentium® 4 and Celeron D can be detected automatically.

3.2 Main Memory

3307760 provides two DDR2-SDRAM DIMM sockets to support dual-channel & single channel DDR2 memory interface. The maximum memory size can be up to 4 GB, memory frequency includes 800/667/533. Auto detects memory clock, which is according to BIOS CMOS settings.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be either one double-sided DIMM in either one DIMM socket or two single-sided DIMM in both sockets.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install memory module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Dual Channel DDR2 DIMMs

Dual Channel DDR2 memory technology doubles the bandwidth of memory bus. Adequate or higher bandwidth of memory than processor would increase system performance. To enable Dual Channel DDR2 memory technology, install two identical memory modules in both memory sockets is required. Following tables show bandwidth information of different processor and memory configurations.

CPU FSB	Bandwidth
1066MHz	8.5 GB/s
800MHz	6.4GB/s
533MHz	4.2GB/s

Memory Frequency	Dual Channel DDR2 Bandwidth	Single Channel DDR2 Bandwidth
800MHz	25.6 GB/s	12.8 GB/s
667MHz	21.2 GB/s	10.6 GB/s
533MHz	16.8 GB/s	8.4 GB/s

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade system performance without acquiring technical information.

Memory frequency / CPU FSB synchronization

3307760 series support different memory frequencies depending on the CPU front side bus and the type of DDR2 DIMM.

CPU FSB	Memory Frequency
1066MHz	800/667/533MHz
800MHz	667/533MHz
533MHz	533MHz

3.3 Installing the Single Board Computer

To install your 3307760 into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place 3307760 into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism. Otherwise, the system might be unstable or do not work due to bad contact of PICMG 1.3 PCI plus.

Note:
Please refer since section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable CMOS Clear Function hardware circuit by putting jumpers at proper position.

JP4	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS contents

To correctly operate CMOS Clear function, users must turn off the system, move JP4 jumper to short pin 2 and 3. To clear CMOS contents, please turn the power back on and turn it off again for AT system, or press the toggle switch a few times for ATX system. Move the JP4 back to 1-2 position (Normal Operation) and start the system. System will then produce a "CMOS Check Sum Error" message and hold up. Users may then follow the displayed message to load BIOS default setting.

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

3307760 allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to Winbond W83627EHG data sheet.

There are two PNP I/O port DDR2 that can be used to configure WDT,
1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
// Enter Extended Function Mode
outp(0x002E, 0x87);
outp(0x002E, 0x87);
// Assign Pin 77 to be a WDTO, 0 write to    CR2D:Bit0
outp(0x002E, 0x2D);
outp(0x002F, inp(0x002F) & 0xEF);
// Select Logic Device 8
outp(0x002E, 0x07);
outp(0x002F, 0x08);
// Active Logic Device 8
outp(0x002E, 0x30);
outp(0x002F, 0x01);
```

```
// Select Count Mode
outp(0x002E, 0xF5);
outp(0x002F, (inp(0x002F) & 0xF7) | ( Count-mode Register  & 0x08));
// Specify Time-out Value
outp(0x002E, 0xF6);
outp(0x002F,  Time-out Value Register );
// Disable WDT reset by keyboard/mouse interrupts
outp(0x002E, 0xF7);
outp(0x002F, 0x00);
// Exit Extended Function Mode
outp(0x002E, 0xAA);
```

Definitions of Variables:

Value of Count-mode Register:
1) 0x00 -- Count down in seconds (Bit3=0)
2) 0x08 -- Count down in minutes (Bit3=1)
Value of Time-out Value Register:
1) 0x00 -- Time-out Disable
2) 0x01~0xFF -- Value for counting down

3.6 SMBus

The System Management Bus is a two-wire interface through which simple power-related chips can communicate with rest of the system. It uses I2C as its backbone.

A system using SMBus passes messages to and from devices instead of tripping individual control lines. With the SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

The SMBus may share the same host device and physical bus as ACCESS bus components provided that an appropriate electrical bridge is provided between the interval SMB devices and external ACCESS bus devices.

3.7 On-Board USB 2.0 Controller

Drivers Support

Please find Intel® ICH8R USB driver in /USB20 directory of 3307760 CD-title. The drivers support Windows-2000/XP.

3.8 GPIO

The 3307760 provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.8.1 Pin assignment

J46: General Purpose I/O Connector

PIN No.	Signal Description
1	General Purpose I/O Port 1 (GPIO10)
2	General Purpose I/O Port 1 (GPIO14)
3	General Purpose I/O Port 1 (GPIO11)
4	General Purpose I/O Port 1 (GPIO15)
5	General Purpose I/O Port 1 (GPIO12)
6	General Purpose I/O Port 1 (GPIO16)
7	General Purpose I/O Port 1 (GPIO13)
8	General Purpose I/O Port 1 (GPIO17)
9	Ground
10	+5V

All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each source sink capacity up to 12mA.

3.8.2 3307760 GPIO Programming Guide

There are 8 GPIO pins on 3307760 series. These GPIO pins are from SUPER I/O (W83627EHG) GPIO pins, and can be programmed as Input or Output direction.

J46 pin header is for 8 GPIO pins and its pin assignment as following :

J46_Pin1=GPIO1:from SUPER I/O_GPIO 10 with Ext. 4.7K PH
J46_Pin2=GPIO2:from SUPER I/O_GPIO 14 with Ext. 4.7K PH
J46_Pin3=GPIO3:from SUPER I/O_GPIO 11 with Ext. 4.7K PH
J46_Pin4=GPIO4:from SUPER I/O_GPIO 15 with Ext. 4.7K PH
J46_Pin6=GPIO5:from SUPER I/O_GPIO 12 with Ext. 4.7K PH
J46_Pin7=GPIO6:from SUPER I/O_GPIO 16 with Ext. 4.7K PH
J46_Pin8=GPIO7:from SUPER I/O_GPIO 13 with Ext. 4.7K PH
J46_Pin9=GPIO8:from SUPER I/O_GPIO17 with Ext. 4.7K PH

<<<<< Be careful Pin9=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of W83627EHG needed to be programmed to control the GPIO direction, and status (GPI)/value (GPO). CR00h ~ CR2F are common (global) registers to all Logical Devices (LD) in W83627EHG. CR07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO10~17 registers.

Programming Guide:
Step1: LD7_CR07h.P [07h]; Point to LD7
Step2: LD7_CR30h_Bit0.P1; Enable LD7
Step3: CR F3h_Bit [7.0]. P [1,1,1,1,1,1,1]; to select multiplexed pins as GPIO10~17 pins
Step4: Select GPIO direction, Get Status or output value.

LD7_CRF0h; GPIO17 ~ 10 direction, 1 = input, 0 = output pin
LD7_CRF2h.P [00h]; Let CRF1 (GPIO data port) non-invert to prevent from confusion
LD7_CRF1h; GPIO17~10 data port, for input pin, get status from the related bit, for output pin, write value to the related bit.

For example,

LD7_CRF0h_Bit4.P0; Let GPIO14 as output pin
LD7_CRF2h_Bit4.P0; Let CRF1_Bit4 non-inverted
LD7_CRF1h_Bit4.P0; Output "0" to GPIO14 pin (J46_Pin2)
LD7_CRF0h_Bit0.P1; Let GPIO10 as input pin
LD7_CRF2h_Bit0.P0; Let CRF1_Bit0 non-inverted
Read LD7_CRF1h_Bit0; Read the status from GPIO10 pin (J46_Pin1)

How to access W83627EHG CR?

In 3307760, the EFER = 002Eh, and EFDR = 002Fh.
EFER and EFDR are 2 IO ports needed to access W83627EHG CR.
EFER is the Index Port, EFDR is the Data Port.
CR index number needs to be written into EFER first,
Then the data will be read/written from/to EFDR.

To R/W W83627EHG CR, it is needed to Enter/Enable Configuration Mode first. When completing the programming, it is suggested to Exit/Disable Configuration Mode.

Enter Configuration Mode: Write 87h to IO port EFER twice.
Exit Configuration Mode: Write AAh to IO port EFER.

3.8.3 Example

The example of program for GPIO test as following is based on J46 1-2, 3-4, 5-6,7-8 short.

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define Superio_Addr        0x2e
/* #define DEBUG                        1 */

void enter_Superio_CFG(void)
{
      outportb(Superio_Addr, 0x87);
      outportb(Superio_Addr, 0x87);
}

void exit_Superio_CFG(void)
{
      outportb(Superio_Addr, 0xAA);
}

void Set_CFG(unsigned char Addr,unsigned char Value)
{
   unsigned char d;
      outportb(Superio_Addr, Addr);
      delay(2);
      outportb(Superio_Addr +1, Value);
#ifdef DEBUG
      d = inportb(Superio_Addr+1);
      printf("\nWrite %x to CR%x, read back is:%x",Value,Addr,d);
#endif /*DEBUG*/
      delay(2);
}
```

```
unsigned char Get_CFG(unsigned char Addr)
{
   unsigned char d;
      outportb(Superio_Addr, Addr);
      delay(2);
      d = inportb(Superio_Addr+1);
#ifdef DEBUG
      printf("\nGet data %x from CR%x",d,Addr);
#endif /*DEBUG*/
      delay(2);
      return(d);
}

int main(void)
{
      unsigned char d;

      printf("\n3307760 GPIO TEST Program R1.0");
      enter_Superio_CFG();
      /* CR29 B0 = 0 selet GPIO Port 1*/
      d = Get_CFG(0x29);
      d = d | 0x01;
      Set_CFG(0x29, d);
      /* IO test loop 1 */
      /* Set GPIO Port 1 Enable */
      Set_CFG(0x07, 0x07);     /* Select logic device 07*/
      Set_CFG(0x30, 0x01);     /* Enable GPIO Port 1 */
      Set_CFG(0xF2, 0x00);
      Set_CFG(0xF3, 0x00);
      Set_CFG(0xF0, 0xF0);     /* GPIO Port 1 B7-4 is input, B3-0 is output */

      Set_CFG(0x07, 0x07);     /* Select logic device 07*/
      Set_CFG(0xF1, 0x0e);     /* GP10 -> ~GP14 */
      d = Get_CFG(0xF1);                  /* get GPIO Port 1 data */
      d = d & 0xF0;
      if (d != 0xe0 )
      {
         printf("\nGP10 -> GP14 test fail !!!\n\n");
         Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
         exit(1);
      }
```

```
Set_CFG(0x07, 0x07);     /* Select logic device 07*/
Set_CFG(0xF1, 0x0d);     /* GP11 -> ~GP15 */
d = Get_CFG(0xF1);                    /* get GPIO Port 1 data */
d = d & 0xF0;
if (d != 0xd0 )
{
   printf("\nGP11 -> GP15 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
Set_CFG(0x07, 0x07);     /* Select logic device 07*/
Set_CFG(0xF1, 0x0b);     /* GP12 -> ~GP16 */
d = Get_CFG(0xF1);                    /* get GPIO Port 1 data */
d = d & 0xF0;
if (d != 0xb0 )
{
   printf("\nGP12 -> GP16 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
Set_CFG(0x07, 0x07);     /* Select logic device 07*/
Set_CFG(0xF1, 0x07);     /* GP13 -> ~GP17 */
d = Get_CFG(0xF1);                    /* get GPIO Port 1 data */
d = d & 0xF0;
if (d != 0x70 )
{
   printf("\nGP13 -> GP17 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
/* IO test loop 2 */
/* Set GPIO Port 1 Enable */
Set_CFG(0x07, 0x07);     /* Select logic device 07*/
Set_CFG(0x30, 0x01);     /* Enable GPIO Port 1 */
Set_CFG(0xF0, 0x0F);     /* GPIO Port 1 B7-4 is output, B3-0 is input */
```

```
Set_CFG(0x07, 0x07);    /* Select logic device 07*/
Set_CFG(0xF1, 0xe0);    /* GP14 -> ~GP10 */
d = Get_CFG(0xF1);                  /* get GPIO Port 1 data */
d = d & 0x0F;
if (d != 0x0e )
{
   printf("\nGP14 -> GP10 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}

Set_CFG(0x07, 0x07);    /* Select logic device 07*/
Set_CFG(0xF1, 0xd0);    /* GP15 -> ~GP11 */
d = Get_CFG(0xF1);                  /* get GPIO Port 1 data */
d = d & 0x0F;
if (d != 0x0d )
{
   printf("\nGP15 -> GP11 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
Set_CFG(0x07, 0x07);    /* Select logic device 07*/
Set_CFG(0xF1, 0xb0);    /* GP16 -> ~GP12 */
d = Get_CFG(0xF1);                  /* get GPIO Port 1 data */
d = d & 0x0F;
if (d != 0x0b )
{
   printf("\nGP16 -> GP12 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
Set_CFG(0x07, 0x07);    /* Select logic device 07*/
Set_CFG(0xF1, 0x70);    /* GP17 -> ~GP13 */
d = Get_CFG(0xF1);                  /* get GPIO Port 1 data */
d = d & 0x0F;
if (d != 0x07 )
{
   printf("\nGP17 -> GP13 test fail !!!\n\n");
   Set_CFG(0xF0, 0xff);  /* GPIO Port 1 is input */
   exit(1);
}
```

```
        Set_CFG(0xF0, 0xff);      /* GPIO Port 1 is input */
        printf("\nGPIO TEST PASS !\n\n");
        return(0);
    }
```

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Device Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0700-0483	16K	DOS
0484-053F	2.9K	Program Area
0540-9EFE	614K	[Available]
9EFE-9EFE	0.1K	Unused
= Conventional memory ends at 640K =		
9F00-9FBF	3K	Extended BIOS Area
9FC0-9FFF	1K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CAFF	44K	Video ROM
CB00-CC49	5.2K	Unused
CC4A-CFFF	14K	High RAM
D000-DFFF	64K	Page Frame
E000-EEFF	60K	Unused
EF00-EFFF	4K	ROM
F000-FFFF	64K	System ROM
HMA	64K	First 64K Extended

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	Unassigned	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	Unassigned	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unassigned	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	Unassigned	Usable IRQ
IRQ 10	Unassigned	Usable IRQ
IRQ 11	Unassigned	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	Unassigned	Usable IRQ

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support your products, projects and business.

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