



integration with integrity

User's Manual

Single Board Computer 3307780

Version 1.0, 2006

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Appendix A

Appendix B

How to Use This Manual

The manual describes how to configure your 3307780 system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

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Chapter 1

System Overview

1.1 Introduction

PCI Express x16 expansion interface and High reliability are two major reasons that PICMG 1.3 Single Host Board (SHB) 3307780 was developed.

The first two PCI Express chipsets that Intel® EID introduced to the world is 915GV & 915GM. Though 915GV supports powerful Intel® Pentium® 4/Celeron D processor but it does not support PCI Express x16 interface which is latest expansion interface of graphics card. Many applications are looking for high-end graphics card but in vain with PCIMG standards such as PICMG 1.0/1.2 since the previous graphics card interface, AGP external expansion does not support by those form factor. The limitation finally resolved by presenting of PICMG 1.3. With this standard, SHB can support external graphics card, therefore, user can choose the most wonderful graphics card for their applications. As a result, 915GM was selected to be the kernel of 3307780.

The SHB does not only provide PCI Express x16 expansion capability but also adopts Pentium® M/Celeron M processor that only generates less than half TDP (Thermal Design Power) of Pentium® 4/Celeron D processor. That benefits to power saving as well as weight and noise of processor cooler. The reliability of the system dramatically increased as a return.

3307780 features:

- Support socket mPGA479M type, 400/533MHz FSB, Pentium® M and Celeron M processor
- Two SODIMM sockets provide up to 2GB DDR2 400/533 system memory expansion capability in dual channel
- 915GM integrated graphics engine - GMA 900
- Equipped dual Gigabit Ethernet
- Audio in/out, Watch-dog timer, Type II CompactFlash socket, 8 USB 2.0 ports (two ports dedicated to keyboard & mouse)
- Support four PCI Express x1, one PCI Express x16 and four PCI expansion via backplane

1.2 Check List

The 3307780 package should cover the following basic items:

- ✓ One 3307780 single host board
- ✓ One dual Serial ports cable kit
- ✓ One Parallel port cable kit
- ✓ One FDC cable
- ✓ One IDE cable
- ✓ Two 7-pin SATA signal cables
- ✓ One Installation Resources CD-Title
- ✓ One booklet of 3307780

Optional: One bracket with PS/2 keyboard and mouse

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**
 - Intel® Pentium® M/Celeron M Processor
 - FSB: 533/400MHz
- **BIOS**

Phoenix (Award) system BIOS with 4Mb Flash ROM with easy upgrade function
ACPI, DMI, Green function and Plug and Play Compatible
- **Main Memory**
 - Support single channel DDR2 memory interface
 - Non-ECC, non-buffered DIMMs only
 - Two SODIMM sockets support 533/400 DDR2-SDRAM up to 2GB System Memory
- **L2 Cache Memory**

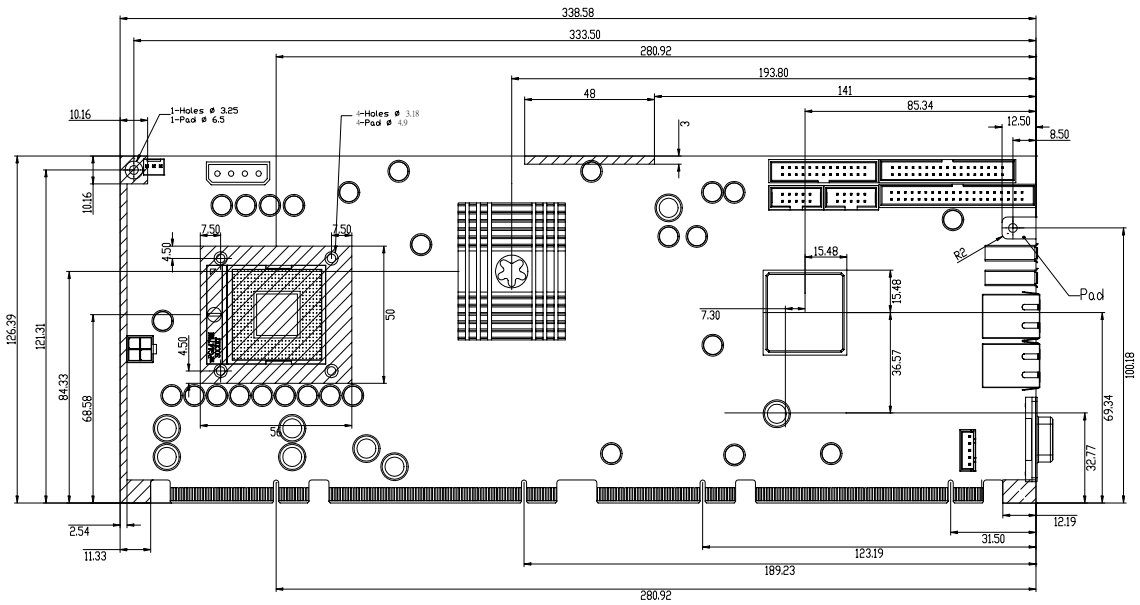
Built-in Processor
- **Chipset**

Intel® 915GM GMCH and ICH6 chipset
- **Bus Interface**
 - Follow PICMG 1.3 Rev 1.0 standard (PCI Express and PCI)
 - Support one PCI Express x16 through backplane
 - Support four PCI Express x1 through backplane
 - Support for PCI devices through backplane

- **IDE Interface**
Support one enhanced IDE port up to two HDD devices with PIO mode 4 and Ultra DMA/33/66/100 mode transfer and Bus Master feature
- **Floppy Drive Interface**
Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD
- **Serial Ports**
Support two high-speed 16C550 compatible UARTs with 16-byte T/R FIFOs
- **IR Interface**
Support one 6-pin header for serial Standard Infrared wireless communication
- **Parallel Port**
Support one parallel port with SPP, EPP and ECP modes
- **USB Interface**
Support eight USB (Universal Serial Bus) ports for high-speed I/O peripheral devices
- **PS/2 Mouse and Keyboard Interface**
Support one 8-pin connector for external PS/2 keyboard/mouse connection
- **Auxiliary I/O Interfaces**
System reset switch, external speaker, Keyboard lock and HDD active LED, etc
- **Real Time Clock/Calendar (RTC)**
Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention
- **Watchdog Timer**
 - Support WDT function through software programming for enable/disable and interval setting
 - Generate system reset
- **CompactFlash**
 - True IDE mode, compatibles with the ATA/ATAPI-4 specification
 - One Type II CF socket on secondary IDE channel for supporting up to 1GB memory
 - Support DMA mode
 - Bootable for no drives on primary channel
- **On-board VGA**
 - GMCH integrated graphics, 333MHz core frequency; share system memory up to 224MB for system with greater than or equal to 512MB of system memory
- **On-board Ethernet LAN**
Marvell PCI interface based Gigabit Ethernet to support RJ-45 connector
- **High Driving GPIO**
Support 8 programmable high driving GPIO

- **Cooling Fans**
Support two 3-pin header for CPU and system
- **System Monitoring Feature**
Monitor CPU temperature, system temperature and major power sources, etc
- **Bracket**
Support dual Ethernet port with 2 indicators, dual USB ports and one CRT port
- **Outline Dimension (L X W):**
338.5mm (13.33") X 122mm (4.8")
- **Power Requirements:**
 - +12V@ 1.59A
 - +5V @ 3.34A
 - Test configuration:
 - CPU: Intel Pentium M (Dothan) - 1.6GHz/400MHz FSB/2MB L2 Cache
 - Memory: Apacer DDR2-SODIMM 512MBx2 UNB PC4300 CL4
 - Primary Master IDE HDD: Seagate-ST320413A
 - OS: Microsoft Windows 2000 Professional + SP4
 - Test Programs: Burning Test V4.0
 - Run Time: 10 minutes
- **Operating Temperature:**
-5°C ~ 60°C (23°F ~ 140°F)
- **Storage Temperature:**
-20°C ~ 80°C
- **Relative Humidity:**
0% ~ 95%, non-condensing

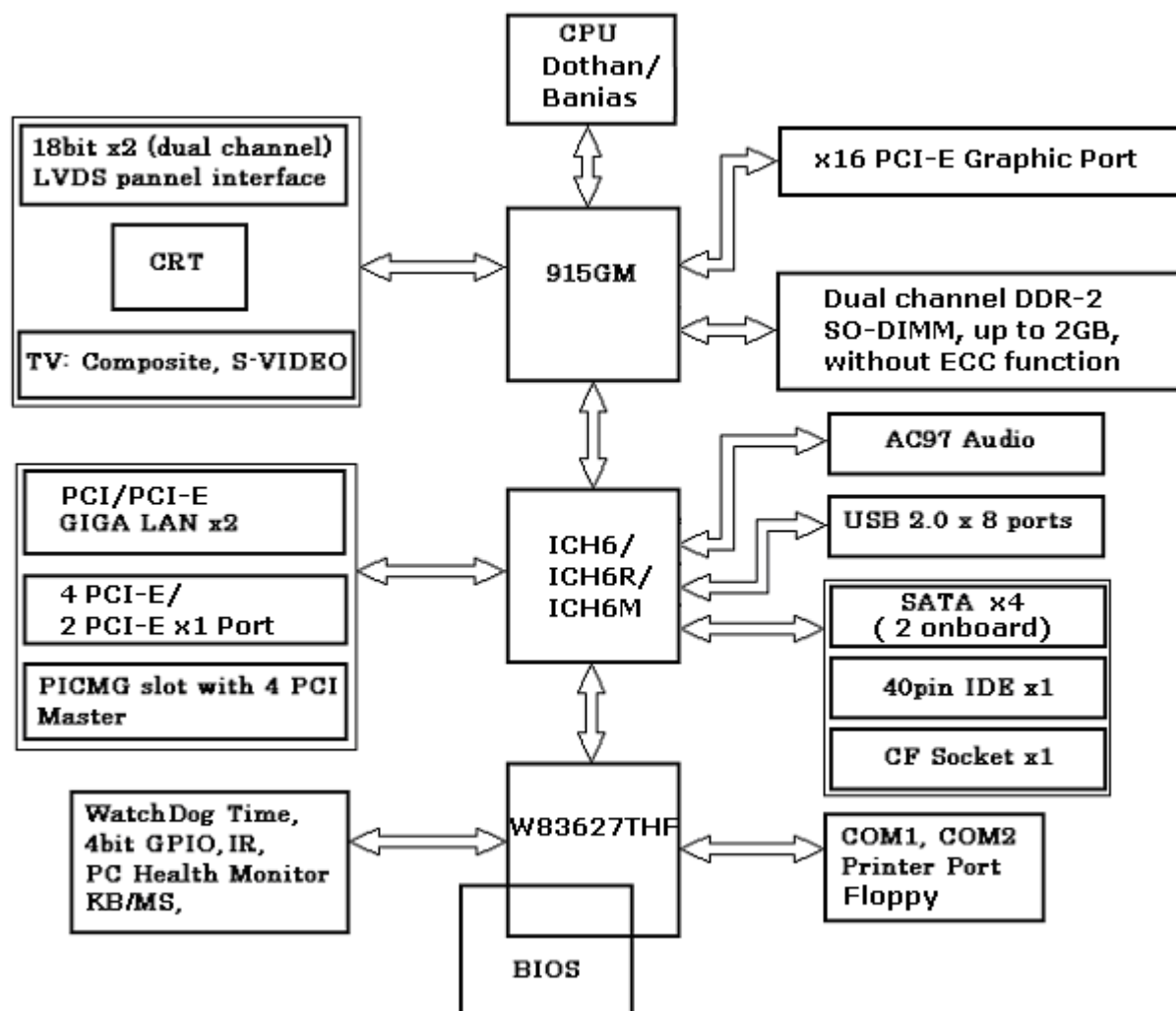
1.3.1 Mechanical Drawing



1.4 System Architecture

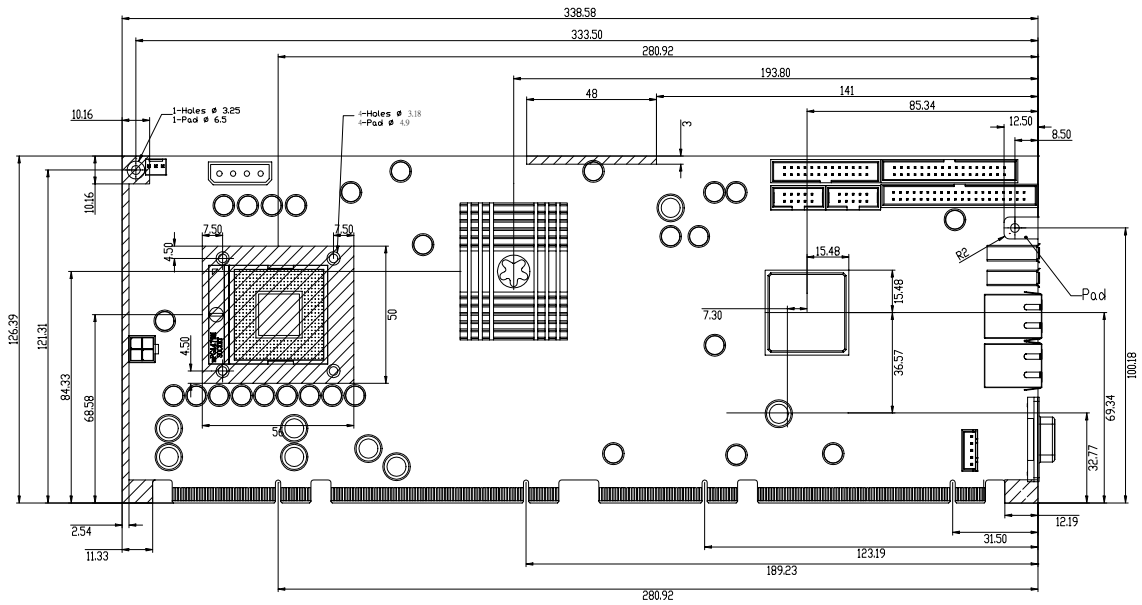
3307780 include Intel® chipset 915GM support Pentium® M/Celeron M processor, DDR2 SDRAM, 2D/3D graphics display, PCI Express x16 and ICH6 supports PCI Express x1 & PCI bus interface, APM, ACPI compliant power management, USB port, SMBus communication, Ultra DMA 33/66/100 IDE channel and SATA ports.

Super I/O chip, W83627THF is responsible for PS/2 keyboard/mouse, UARTs, FDC, hardware monitor, Parallel, Watch Dog Timer and Infrared interface.



3307780 System Block Diagram

1.3.1 Mechanical Drawing



JP1: LVDS Panel VDD input voltage selection

JP1	Function
1-2 short	VDD=3.3V ★
2-3 short	VDD=5V

Note:

Wrong voltage selection may damage the LVDS panel. Please survey LVDS panel's VDD before setup this jumper setting.

JP2A: LVDS panel backlight inverter enable signal voltage level selection

JP2A	Function
1-3 short	Backlight enable level=3.3V ★
3-5 short	Backlight enable level=5V.

Note:

Wrong voltage selection may damage the inverter. Please survey the inverter's voltage input before setup this jumper setting.

JP2B: CPU VCCA voltage input

JP2B	Function
2-4 short	VCCA=1.8V (Banias)
4-6 short	VCCA=1.5V (Dothan) ★

Note:

Wrong voltage selection may damage the CPU. Please survey the CPU's type before setup this jumper setting.

JP2C: PCI-E x16 graphic port enable/disable

JP2C	Function
7-8 short	Reserved
7-8 open	PCI-E x16 graphic port enabled ★

JP2D: DDR2 memory frequency selection

JP2D	Function
9-10 open 11-12 open	Reserved
9-10 open 11-12 short	The memory module is DDR2 400 ★
9-10 short 11-12 open	The memory module is DDR2 533
9-10 short 11-12 short	Reserved

JP3 : VIO Voltage selection

JP3	Function
1-2 short	Without Backplane
2-3 short	Have Backplane ★

JP4 : CPU FSB frequency selection

JP4	Function
1-2 short	CPU FSB frequency=400MHz ★
2-3 short	CPU FSB frequency=533MHz

Note:

The DDR2 frequency is followed the CPU FSB frequency. For example, the DDR2 module populated is DDR2 533, the CPU must be 533MHz FSB. Please use same frequency of memory module and CPU. Neither CPU/DDR=533/400 nor 400/533 are allowed. This is the limitation of 915GM chipset.

JP5 : COM2 Communication Protocol selection

JP5	Function
5-6,9-11,10-12,15-17,16-18 short	RS-232 ★
3-4,7-9,8-10,13-15,14-16,21-22 short	RS -422
1-2,7-9,8-10,19-20	RS-485

JP6 : CMOS RAM charge/discharge setup

JP6	Function
1-2 short	Clear CMOS
2-3 short	Charge ★

JP7 : LVDS panel type selection

JP7	Function
1-2, 3-4, 5-6, 7-8	Panel type
Short, short, short, short	Setup by "CMOS setup" in the "chipset feature" ★
Open, short, short, short	640x480 18bit single channel
Short, open, short, short	800x600 18bit single channel
Open, open, short, short	1024x768 18bit single channel
Short, short, open, short	Reserved
Open, short, open, short	Reserved
Short, open, open, short	Reserved
Open, open, open, short	1400x1050 18bit dual channel
Short, short, short, open	Reserved
Open, short, short, open	Reserved
Short, open, short, open	Reserved
Open, open, short, open	Reserved
Short, short, open, open	Reserved
Open, short, open, open	Reserved
Short, open, open, open	Reserved
Open, open, open, open	Reserved

JP8 : Reserved jumper

JP8	Function
Short	Reserved
Open	Reserved

JP9 : ATX/AT Mode Function selection

JP9	Function
1-2 Open	ATX Mode ★
1-2 short	AT Power Emulation

Note:

"AT Power Emulation" means the 3307780 is able to be auto power up once power cord is plugged in ATX power supply. However, user need set BIOS setup menu "PWRON after PWR FAIL" to "ON" if you need auto power up function.

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors (Figure 2-1)

Connector Function List

Connector	Function	Remark
J1	LVDS panel backlight inverter power connector	
J2, J31	+12V DC FAN connector	
J3	I2C connector	
J4	LVDS panel connector	
J5	Audio connector	
J6	Front panel connector	
J7	Parallel port connector	
J8	Floppy disk connector	
J9	WOL connector	
J10	CD-IN connector	
J11	External PC speaker connector	
J12	External thermal sensor connector	
J13	+12V and +5V power input connector	
J14	TV out connector	
J15	IDE connector	
J16	COM2 connector	
J17	COM1 connector	
J18	IR connector	
J19	SATA connector	
J20	General purpose I/O connector	
J21	SATA 0 connector	
J22	USB port 0 connector	
J23	USB port 1 connector	
J24	Ethernet port 0	
J25	+12V power input connector	
J26	Ethernet port 1 connector	
J27	Ethernet port0 external status LED connector	
J28	Ethernet port1 external status LED connector	
J29	USB port 2 and port 3 connector	
J30	CRT connector	
J32	External Keyboard connector	
J33	Keyboard and mouse connector	
J34	Compact flash card socket	
DIMM1	Channel A DDR2 SO-DIMM connector	
DIMM2	Channel B DDR2 SO-DIMM connector	
CPU	479 pin CPU socket.	

Pin Assignments of Connectors**J1: LVDS Panel Back Light Inverter Power Connector**

PIN No.	Signal Description
1	+5V
2	GND
3	+12V
4	GND
5	Back Light Enable signal. Active high.

J2, J31: 12V DC Fan Connector

PIN No.	Signal Description
1	GND
2	Power pin
3	Speed pulse output

J3: I2C Connector

PIN No.	Signal Description
1	I2C clock
2	NC
3	GND
4	I2C data
5	5V

J4: LVDS Panel Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Panel VDD	2	Panel VDD
3	CHA DATA0+	4	CHA DATA0-
5	CHA DATA1+	6	CHA DATA1-
7	CHA DATA2+	8	CHA DATA2-
9	NC	10	NC
11	CHA CLOCK+	12	CHA CLOCK-
13	NC	14	NC
15	GND	16	GND
17	CHB DATA0+	18	CHB DATA0-
19	CHB DATA1+	20	CHB DATA1-
21	CHB DATA2+	22	CHB DATA2-
23	NC	24	NC

25	CHB CLOCK+	26	CHB CLOCK-
27	NC	28	NC
29	GND	30	GND

Notes:

- 1) The signals of LVDS upper channel will be only used in dual-channel LVDS mode.
- 2) This panel connector (J4) should be accompanied with LVDS Panel Voltage jumper setting (JP1)
- 3) In general, lower channel equals odd channel and upper channel equals even channel for different panel description.

J5: Audio Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	MIC	2	Ground
3	Line in channel L	4	Ground
5	Line in channel R	6	Ground
7	Line out channel L	8	Ground
9	Line out channel R	10	NC

Note:

The Reference Voltage on MIC signal offers 2.25V~2.75V with 5mA drive.

J6: Front Panel Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	5Vsb pull up (power LED+)	2	Power LED-
3	3V pull up (HDD LED+)	4	HDD LED-
5	NC	6	NC
7	3Vsb pull up (reset button +)	8	GND (Reset button -)

Notes:

- 1) The Power button connector is on the PICMG 1.3 back plane only. It is unavailable in the single board computer.
- 2) The reset buttons are resides on both back plane and this SBC. These 2 connectors were wired together. And, anyone of them can cause a system reset independent.

J7: Printer Port Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	STROBE#	2	AFD#
3	DATA0	4	ERR#
5	DATA1	6	INIT#
7	DATA2	8	SLIN#
9	DATA3	10	GND
11	DATA4	12	GND
13	DATA5	14	GND
15	DATA6	16	GND
17	DATA7	18	GND
19	ACK#	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

J8: FDC Interface Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Drive density select bit 0
3	Ground	4	NC
5	Ground	6	NC
7	Ground	8	Index
9	Ground	10	MOA#, motor A on
11	Ground	12	NC
13	Ground	14	Drive select A
15	Ground	16	NC
17	Ground	18	Direction of step motor
19	Ground	20	STEP#, move head to another track
21	Ground	22	Write data
23	Ground	24	Write enable
25	Ground	26	Track 0
27	Ground	28	Write protection
29	NC	30	Read data
31	Ground	32	Head select
33	NC	34	Diskette change

J9: WOL (Wake On Lan) Connector

PIN No.	Signal Description
1	5Vsb
2	GND
3	Wake up signal. Active high.

Notes:

- 1) This connector was dedicated to some Ethernet card, the Ethernet card without wake up signals on the PCI gold finger. Such a card may have one white connector same as J9. Please survey the Ethernet card's WOL function and connector.
- 2) Please survey the pin assignment of Ethernet card is same as J9. Different pin assignment may damage either Ethernet card or SBC.

J10: CD-IN Connector

PIN No.	Signal Description
1	CD-IN Left
2	CD-Ground
3	CD-Ground
4	CD-IN Right

J11: PC speaker Connector

PIN No.	Signal Description
1	Speaker (-)
2	NC
3	NC
4	Speaker (+). 5V

J12: External thermal sensor Connector

PIN No.	Signal Description
1	Thermal sensor pin 1
2	Thermal sensor pin 2

Notes:

- 1) Support thermistor with thermal sensor only.
- 2) The thermal data of this sensor can be read from the "PC Health" in the CMOS setup.
- 3) The thermal data of this connector is not available in CMOS setup, if the thermal sensor was not attached.
- 4) The thermal data of this connector is not available in CMOS setup, if the temperature over 120°C.

- 5) An external thermistor can be connected these two pins for temperature monitoring remotely, such as chassis ambient temperature, etc. Normally, the resistance selected for thermistor should be 10K Ω at 25°C.

J13: +12V and +5V power input Connector

PIN No.	Signal Description
1	+12V
2	Ground
3	Ground
4	+5V

J14: TV Out Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	TVDAC A
3	TVDAC B	4	TVDAC C
5	GND	6	NC

Note:

TVDAC_A: COMPOSITE VIDEO

TVDAC_B: S-VIDEO LUMINANCE

TVDAC_C: S-VIDEO CHROMINANCE

J15: IDE Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	RESET#	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	Key pin
21	DREQ	22	GND
23	DIOW#	24	GND
25	DIOR#	26	GND
27	DIORDY	28	Pull down
29	DACK#	30	GND
31	IRQ14	32	NC

33	DA1	34	DETECT
35	DA0	36	DA2
37	DCS1#	38	DCS#3
39	IDE ACTIVE#	40	GND

J16 & J17: COM1 & COM2 connector

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	RI
5	GND		

Note:

COM1 under COM2.

J18: IR Connector

PIN No.	Signal Description
1	+5V
2	Reserved
3	IRRX
4	Ground
5	IRTX
6	NC (Key pin)

J19 & J21: SATA Connector

PIN No.	Signal Description
1	Ground
2	SATA TX+
3	SATA TX-
4	Ground
5	SATA RX-
6	SATA RX+
7	Ground

J20: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Input bit 0	2	Output bit 0
3	Input bit 1	4	Output bit 1
5	Input bit 2	6	Output bit 2
7	Input bit 3	8	Output bit 3
9	GND	10	5V

Note:

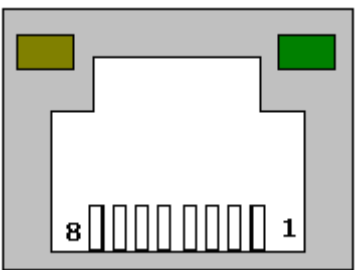
All General Purpose I/O ports can only adapt standard TTL \pm 5% signal level (0V/5V).

J22 & J23: USB Connector

PIN No.	Signal Description
1	USB power (+5V)
2	USB D-
3	USB D+
4	USB ground

J24 & J26: Ethernet port Connector

RJ-45 PIN No.	Signal Description
1	MDIA+
2	MDIA-
3	MDIB+
4	MDIC+
5	MDIC-
6	MDIB-
7	MDID+
8	MDID-


Note:

Only J26 support LAN wake up function.

J25: +12V power input Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	GND
3	+12V	4	+12V

J27, J28: Ethernet port 0 and port 1 external status LED connector

PIN No.	Signal Description	PIN No.	Signal Description
1	LINK LED (-)	2	LINK LED (+)
3	ACTIVE LED (-)	4	ACTIVE LED(+)
5	10/100 speed LED (-)	6	10/100 speed LED (+)
7	1000 speed LED (-)	8	1000 speed LED (+)

J29: USB Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	NC	2	USB power (5V)
3	USB GND	4	USB DATA A-
5	USB DATA B+	6	USB DATA A+
7	USB DATA B-	8	USB GND
9	USB power (5V)	10	Chassis ground

Note:

The other 4 USB port are reside on the PICMG1.3 back plane.

J30: VGA Connector

PIN No.	Signal Description	PIN No.	Signal Description	PIN No.	Signal Description
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	DDC DATA
3	BLUE	8	GND	13	HSYNC
4	NC	9	NC	14	VSYNC
5	GND	10	GND	15	DDC CLOCK

J32: External keyboard Connector

PIN No.	Signal Description
1	KB clock
2	KB data
3	NC
4	KB ground
5	KB VCC

J33: PS/2 Keyboard & Mouse Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Keyboard data	2	Mouse data
3	KB/MS ground	4	KB/MS VCC (+5V)
5	Keyboard clock	6	Mouse clock
7	NC (key)	8	NC (key)

J34: Compact Flash Socket

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	26	NC
2	Data 3	27	Data 11
3	Data 4	28	Data 12
4	Data 5	29	Data 13
5	Data 6	30	Data 14
6	Data 7	31	Data 15
7	Select 0	32	Select 1
8	Ground	33	NC
9	Ground	34	IO Read
10	Ground	35	IO Write
11	Ground	36	Pull Up to +5V
12	Ground	37	IRQ 14
13	+5V	38	+5V
14	Ground	39	Pull down
15	Ground	40	NC
16	Ground	41	Reset
17	Ground	42	IORDY
18	SA2	43	NC
19	SA1	44	Pull Up to +5V
20	SA0	45	IDE Active
21	Data 0	46	Pull Up to +5V
22	Data 1	47	Data 8
23	Data 2	48	Data 9
24	NC	49	Data 10
25	NC	50	Ground

PICMG gold finger pin assignment table

PIN No.	Signal Description	PIN No.	Signal Description
B1	SM bus clock	A1	SM bus data
B2	GND	A2	GND
B3	Reserved	A3	Reserved
B4	Reserved	A4	Reserved
B5	Reserved	A5	PCI-Express wake signal#
B6	Power button	A6	PCI PME#
B7	ATX power good	A7	PS_ON#
B8	Reset button	A8	PCI reset
B9	Reserved	A9	NC
B10	Reserved	A10	PCI-Express configure pin
B11	Reserved	A11	GND
B12	GND	A12	Reserved
B13	PCI-Ex1 channel 0 TX+	A13	GND
B14	PCI-Ex1 channel 0 TX-	A14	GND
B15	GND	A15	PCI-Ex1 channel 0 RX+
B16	GND	A16	PCI-Ex1 channel 0 RX-
B17	PCI-Ex1 channel 1 TX+	A17	GND
B18	PCI-Ex1 channel 1 TX-	A18	GND
B19	GND	A19	PCI-Ex1 channel 1 RX+
B20	GND	A20	PCI-Ex1 channel 1 RX-
B21	PCI-Ex1 channel 2 TX+	A21	GND
B22	PCI-Ex1 channel 2 TX-	A22	GND
B23	GND	A23	PCI-Ex1 channel 2 RX+
B24	GND	A24	PCI-Ex1 channel 2 RX-
B25	PCI-Ex1 channel 3 TX+	A25	GND
B26	PCI-Ex1 channel 3 TX-	A26	GND
B27	GND	A27	PCI-Ex1 channel 3 RX+
B28	GND	A28	PCI-Ex1 channel 3 RX-
B29	CLOCK0+	A29	GND
B30	CLOCK0-	A30	GND
B31	GND	A31	CLOCK1+
B32	Reserved	A32	CLOCK1-
B33	CLOCK2+	A33	GND
B34	CLOCK2-	A34	GND
B35	GND	A35	CLOCK3+
B36	Reserved	A36	CLOCK3-
B37	CLOCK4+	A37	GND
B38	CLOCK4-	A38	GND
B39	GND	A39	Reserved
B40	Reserved	A40	Reserved

B41	Reserved	A41	GND
B42	Reserved	A42	GND
B43	GND	A43	Reserved
B44	GND	A44	Reserved
B45	PCI-Ex16 channel 0 TX+	A45	GND
B46	PCI-Ex16 channel 0 TX-	A46	GND
B47	GND	A47	PCI-Ex16 channel 0 RX+
B48	GND	A48	PCI-Ex16 channel 0 RX-
B49	PCI-Ex16 channel 1 TX+	A49	GND
B50	PCI-Ex16 channel 1 TX-	A50	GND
B51	GND	A51	PCI-Ex16 channel 1 RX+
B52	GND	A52	PCI-Ex16 channel 1 RX-
B53	PCI-Ex16 channel 2 TX+	A53	GND
B54	PCI-Ex16 channel 2 TX-	A54	GND
B55	GND	A55	PCI-Ex16 channel 2 RX+
B56	GND	A56	PCI-Ex16 channel 2 RX-
B57	PCI-Ex16 channel 3 TX+	A57	GND
B58	PCI-Ex16 channel 3 TX-	A58	GND
B59	GND	A59	PCI-Ex16 channel 3 RX+
B60	GND	A60	PCI-Ex16 channel 3 RX-
B61	PCI-Ex16 channel 4 TX+	A61	GND
B62	PCI-Ex16 channel 4 TX-	A62	GND
B63	GND	A63	PCI-Ex16 channel 4 RX+
B64	GND	A64	PCI-Ex16 channel 4 RX-
B65	PCI-Ex16 channel 5 TX+	A65	GND
B66	PCI-Ex16 channel 5 TX-	A66	GND
B67	GND	A67	PCI-Ex16 channel 5 RX+
B68	GND	A68	PCI-Ex16 channel 5 RX-
B69	PCI-Ex16 channel 6 TX+	A69	GND
B70	PCI-Ex16 channel 6 TX-	A70	GND
B71	GND	A71	PCI-Ex16 channel 6 RX+
B72	GND	A72	PCI-Ex16 channel 6 RX-
B73	PCI-Ex16 channel 7 TX+	A73	GND
B74	PCI-Ex16 channel 7 TX-	A74	GND
B75	GND	A75	PCI-Ex16 channel 7 RX+
B76	GND	A76	PCI-Ex16 channel 7 RX-
B77	Reserved	A77	GND
B78	+3.3V	A78	+3.3V
B79	+3.3V	A79	+3.3V
B80	+3.3V	A80	+3.3V
B81	+3.3V	A81	+3.3V
B82	Reserved	A82	Reserved
D1	5VSB	C1	5Vsb

D2	GND	C2	Reserved
D3	PCI-Ex16 channel 8 TX+	C3	GND
D4	PCI-Ex16 channel 8 TX-	C4	GND
D5	GND	C5	PCI-Ex16 channel 8 RX+
D6	GND	C6	PCI-Ex16 channel 8 RX-
D7	PCI-Ex16 channel 9 TX+	C7	GND
D8	PCI-Ex16 channel 9 TX-	C8	GND
D9	GND	C9	PCI-Ex16 channel 9 RX+
D10	GND	C10	PCI-Ex16 channel 9 RX-
D11	Reserved	C11	Reserved
D12	GND	C12	Reserved
D13	PCI-Ex16 channel 10 TX+	C13	GND
D14	PCI-Ex16 channel 10 TX-	C14	GND
D15	GND	C15	PCI-Ex16 channel 10 RX+
D16	GND	C16	PCI-Ex16 channel 10 RX-
D17	PCI-Ex16 channel 11 TX+	C17	GND
D18	PCI-Ex16 channel 11 TX-	C18	GND
D19	GND	C19	PCI-Ex16 channel 11 RX+
D20	GND	C20	PCI-Ex16 channel 11 RX-
D21	PCI-Ex16 channel 12 TX+	C21	GND
D22	PCI-Ex16 channel 12 TX-	C22	GND
D23	GND	C23	PCI-Ex16 channel 12 RX+
D24	GND	C24	PCI-Ex16 channel 12 RX-
D25	PCI-Ex16 channel 13 TX+	C25	GND
D26	PCI-Ex16 channel 13 TX-	C26	GND
D27	GND	C27	PCI-Ex16 channel 13 RX+
D28	GND	C28	PCI-Ex16 channel 13 RX-
D29	PCI-Ex16 channel 14 TX+	C29	GND
D30	PCI-Ex16 channel 14 TX-	C30	GND
D31	GND	C31	PCI-Ex16 channel 14 RX+
D32	GND	C32	PCI-Ex16 channel 14 RX-
D33	PCI-Ex16 channel 15 TX+	C33	GND
D34	PCI-Ex16 channel 15 TX-	C34	GND
D35	GND	C35	PCI-Ex16 channel 10 RX+
D36	GND	C36	PCI-Ex16 channel 10 RX-
D37	Reserved	C37	GND
D38	Reserved	C38	Reserved
D39	GND	C39	GND
D40	GND	C40	GND
D41	GND	C41	GND
D42	GND	C42	GND
D43	GND	C43	GND
D44	+12V	C44	+12V

D45	+12V	C45	+12V
D46	+12V	C46	+12V
D47	+12V	C47	+12V
D48	+12V	C48	+12V
D49	+12V	C49	+12V
F1	USBD4+	E1	GND
F2	USBD4-	E2	GND
F3	GND	E3	USBD5+
F4	GND	E4	USBD5-
F5	USBD6+	E5	GND
F6	USBD6-	E6	GND
F7	GND	E7	USBD7+
F8	GND	E8	USBD7-
F9	USBOC4#	E9	GND
F10	GND	E10	USBOC5#
F11	USBOC6#	E11	GND
F12	GND	E12	USBOC6#
F13	SATA T1+	E13	GND
F14	SATA T1-	E14	GND
F15	GND	E15	SATA R1+
F16	GND	E16	SATA R1-
F17	SATA T3+	E17	GND
F18	SATA T3-	E18	GND
F19	GND	E19	SATA R3+
F20	GND	E20	SATA R3-
F21	Reserved	E21	GND
F22	Reserved	E22	GND
F23	GND	E23	Reserved
F24	GND	E24	Reserved
F25	Reserved	E25	GND
F26	Reserved	E26	GND
F27	GND	E27	Reserved
F28	GND	E28	Reserved
F29	Reserved	E29	GND
F30	Reserved	E30	GND
F31	Reserved	E31	Reserved
F32	Reserved	E32	Reserved
F33	Reserved	E33	Reserved
F34	Reserved	E34	GND
F35	Reserved	E35	GND
F36	GND	E36	Reserved
F37	GND	E37	Reserved

F38	Reserved	E38	GND
F39	Reserved	E39	GND
F40	GND	E40	Reserved
F41	GND	E41	Reserved
F42	+3.3V	E42	+3.3V
F43	+3.3V	E43	+3.3V
F44	+3.3V	E44	+3.3V
F45	+3.3V	E45	+3.3V
F46	+3.3V	E46	+3.3V
F47	+3.3V	E47	+3.3V
F48	+3.3V	E48	+3.3V
F49	+3.3V	E49	+3.3V
F50	+3.3V	E50	+3.3V
F51	GND	E51	GND
F52	GND	E52	GND
F53	GND	E53	GND
F54	GND	E54	GND
F55	GND	E55	GND
F56	GND	E56	GND
F57	GND	E57	GND
F58	GND	E58	GND
F59	+5V	E59	+5V
F60	+5V	E60	+5V
F61	+5V	E61	+5V
F62	+5V	E62	+5V
F63	GND	E63	GND
F64	GND	E64	GND
F65	GND	E65	GND
F66	GND	E66	GND
F67	GND	E67	GND
F68	GND	E68	GND
F69	GND	E69	GND
F70	GND	E70	GND
F71	GND	E71	GND
F72	GND	E72	GND
F73	+12V	E73	+12V
F74	+12V	E74	+12V
F75	+12V	E75	+12V
F76	+12V	E76	+12V
F77	+12V	E77	+12V
F78	+12V	E78	+12V
F79	+12V	E79	+12V
F80	+12V	E80	+12V
F81	+12V	E81	+12V

F82	+12V	E82	+12V
H1	PIRQB#	G1	PIRQ#A
H2	PIRQD#	G2	PIRQ#C
H3	GND	G3	VIO
H4	PREQ#3	G4	PGNT#3
H5	PREQ#2	G5	PGNT#2
H6	PCI RESET#	G6	PGNT#1
H7	PREQ#1	G7	PGNT#0
H8	PREQ#0	G8	SERR#
H9	Pull down to GND	G9	+3.3V
H10	GND	G10	GND
H11	GND	G11	GND
H12	PCICLK2	G12	PCICLK3
H13	GND	G13	+3.3V
H14	PCICLK0	G14	PCICLK1
H15	+3.3V	G15	GND
H16	AD31	G16	GND
H17	AD29	G17	+3.3V
H18	Pull down to ground	G18	AD30
H19	AD27	G19	AD28
H20	AD25	G20	GND
H21	GND	G21	AD26
H22	C/BE#3	G22	AD24
H23	AD23	G23	+3.3V
H24	GND	G24	AD22
H25	AD21	G25	AD20
H26	AD19	G26	Pull down to ground
H27	+5V	G27	AD18
H28	AD17	G28	AD16
H29	C/BE#2	G29	GND
H30	PCI_PRST#	G30	FRAME#
H31	IRDY#	G31	TRDY#
H32	DEVICE SELECT#	G32	+5V
H33	PCI LOCK#	G33	STOP#
H34	PCI ERR#	G34	GND
H35	GND	G35	C/BE#1
H36	PAR	G36	AD14
H37	Pull high to +3.3V	G37	GND
H38	GND	G38	AD12
H39	AD15	G39	AD10
H40	AD13	G40	GND
H41	GND	G41	AD9

H42	AD11	G42	C/BE#0
H43	AD8	G43	GND
H44	GND	G44	AD6
H45	AD7	G45	AD5
H46	AD4	G46	GND
H47	GND	G47	AD2
H48	AD3	G48	AD1
H49	AD0	G49	GND

Chapter 3

System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle WDT operation in software programming.

3.1 Pentium M Processor

Installing mPGA 479M CPU

- 1) Lift the handling lever of CPU socket outwards and upwards to the other end.



- 2) Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place. If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.



- 3) Push down the lever to lock processor chip into the socket once CPU fits.
- 4) Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the mPGA479M socket.

J25: +12V Power input Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GND	2	GND
3	+12V	4	+12V

Note:

You should know Pentium M processor need extra 12V Power source. DON'T FORGET TO CONNECT 4pin 12V connector to J25!

Removing CPU

- 1) Unlock the cooling fan first.
- 2) Lift the lever of CPU socket outwards and upwards to the other end.
- 3) Carefully lifts up the existing CPU to remove it from the socket.
- 4) Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

Configuring System Bus

3307780 will automatically detect the CPU used. CPU speed of Intel Pentium M can be detected automatically.

JP2B : CPU VCCA voltage input

JP2B	Function
2-4 short	VCCA=1.8V (Banias)
4-6 short	VCCA=1.5V (Dothan) ★

Note:

Wrong voltage selection may damage the CPU. Please survey the CPU's type before setup this jumper setting.

JP4: CPU FSB frequency selection

JP4	Function
1-2 short	CPU FSB frequency=400MHz ★
2-3 short	CPU FSB frequency=533MHz

Notes:

- 1) The DDR2 frequency is followed the CPU FSB frequency. For example, the DDR2 module populated is DDR2 533; the CPU must be 533MHz FSB. Please use same frequency of memory module and CPU.
- 2) Neither CPU/DDR=533/400 nor 400/533 are allowed. This is the limitation of 915GM chipset.

3.2 Main Memory

3307780 provides 2 x 200-pin SODIMM sockets (dual channel) support 1.8V DDR2-SDRAM as on-board main memory. The maximum memory size can be up to 2GB. Auto detecting memory clock according to BIOS CMOS settings.

JP2D: DDR2 memory frequency selection

JP2D	Function
9-10 open 11-12 short	The memory module is DDR2 400 ★
9-10 short 11-12 open	The memory module is DDR2 533

Memory frequency / CPU FSB synchronization

3307780 support different memory frequencies depending on the CPU front side bus and the type of DDR II SODIMM.

CPU FSB	Memory Frequency
533MHz	533/400MHz
400MHz	400MHz

JP2C: PCI-E x16 graphic port enable/disable

3307780 support PCI-E by 16 Slot, for PCI-E by 16 VGA Card.

JP2C	Function
7-8 short	Reserved
7-8 open	PCI-E x16 graphic port enabled ★

3.3 Installing the Single Board Computer

To install your 3307780 into standard chassis or proprietary environment, you need to perform the following:

Step 1: Check all jumpers setting on proper position

Step 2: Install and configure CPU and memory module on right position

Step 3: Place 3307780 into the dedicated position in your system

Step 4: Attach cables to existing peripheral devices and secure it

3.4 Clear CMOS Operation

The following table indicates how to enable/disable CMOS Clear Function hardware circuit by putting jumpers at proper position.

JP6: RTC CMOS Clear Jumper Setting

JP6	Process Selection
1-2	Normal Operation ★
2-3	Clear CMOS Contents

To correctly operate CMOS Clear function, users must turn off the system, move JP6 jumper to short pin 2 and 3. To clear CMOS contents, please turn the power back on and turn it off again for AT system, or press the toggle switch a few times for ATX system. Move the JP6 back to 1-2 position (Normal Operation) and start the system. System will then produce a "CMOS Check Sum Error" message and hold up. Users may then follow the displayed message to load BIOS default setting.

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

The 3307780 allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process.

A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately.

To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to Winbond W83627THF data sheet.

There are two PnP I/O port addresses that can be used to configure WDT,

- 1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
- 2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
// Enter Extended Function Mode
outp(0x002E, 0x87);
outp(0x002E, 0x87);
// Assign Pin 89 to be a WDIO
outp(0x002E, 0x2B);
outp(0x002F, inp(0x002F) & 0xEF);
```

```
// Select Logic Device 8
outp(0x002E, 0x07);
outp(0x002F, 0x08);
// Active Logic Device 8
outp(0x002E, 0x30);
outp(0x002F, 0x01);
// Select Count Mode
outp(0x002E, 0xF5);
outp(0x002F, (inp(0x002F) & 0xF7) | (Count-mode Register & 0x08));
// Specify Time-out Value
outp(0x002E, 0xF6);
outp(0x002F, (Time-out Value Register));
// Disable WDT reset by keyboard/mouse interrupts
outp(0x002E, 0xF7);
outp(0x002F, 0x00);
// Exit Extended Function Mode
outp(0x002E, 0xAA);
```

Definitions of Variables:

Value of **Count-mode Register**:

- 1) 0x00 -- Count down in seconds (Bit3=0)
- 2) 0x08 -- Count down in minutes (Bit3=1)

Value of **Time-out Value Register**:

- 1) 0x00 -- Time-out Disable
- 2) 0x01~0xFF -- Value for counting down

3.6 GPIO

The 3307780 provides 4 input/output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

J20 : GPIO Connector from Super I/O



PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO Port10	2	GPIO Port14
3	GPIO Port11	4	GPIO Port15
5	GPIO Port12	6	GPIO Port16
7	GPIO Port13	8	GPIO Port17
9	Ground	10	+5V

Additionally, 4-extra Digital Output ports inversely amplified signals from GPIO ports. There are open-drain buffers, which can offer greater driving capacity up to 100mA.

There are two PnP I/O port addresses that can be used to configure GPIO ports,

- 1) 0x2E - EFER (Extended Function Enable Register, for entering Extended Function Mode)
 - EFIR (Extended Function Index Register, for identifying CR index number)
- 2) 0x2F - EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of GPIOs.

```
// Enter Extended Function Mode
outp(0x002E, 0x87);
outp(0x002E, 0x87);
// Assign Pin121-128 to be GPIO port 1
outp(0x002E, 0x29);
outp(0x002F, 0x7F) ;
// Select Logic Device 7
outp(0x002E, 0x07);
outp(0x002F, 0x07);
// Active Logic Device 7
```

```
outp(0x002E, 0x30);
outp(0x002F, 0xFF);
// Select Inversion Mode
outp(0x002E, 0xF2);

outp(0x002F, (inp(0x002F) & 0x0F) | (Inversion Register & 0xF0));
// Select I/O Mode
outp(0x002E, 0xF0);
outp(0x002F, (inp(0x002F) & 0x0F) | (I/O Selection Register & 0xF0));
// Access GPIO ports
outp(0x002E, 0xF1);
outp(0x002F, (inp(0x002F) & 0x0F) | (Output Data & 0xF0));
or
Input Data = inp(0x002F);
// Exit Extended Function Mode
outp(0x002E, 0xAA);
```

Definitions of Variables:

Each bit in the lower nibble of each Register represents the setting of a GPIO port.

Bit0 vs. GPIO port 1

Bit1 vs. GPIO port 2

Bit2 vs. GPIO port 3

Bit3 vs. GPIO port 4

Bit4 vs. GPIO port 5

Bit5 vs. GPIO port 6

Bit6 vs. GPIO port 7

Bit7 vs. GPIO port 8

Value of **Inversion Register**:

Only high nibble is available for this function.

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in Data Register.

Value of **I/O Selection Register**:

Only high nibble is available for this function.

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

Value of **Output Data**/**Input Data**:

Only high nibble is available for this function.

If a port is assigned to be an output port, then its respective bit can be read/written.

If a port is assigned to be an input port, then its respective bit can be read only.

Notes:

- 1) All the Buffered Digital Outputs are open-drain amplified form corresponding GPIO ports.
- 2) Some other functions may occupy the lower nibble of the registers. Altering any content in lower nibble will be undesired.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Device Description
0000 - 003F	1K	Interrupt Area
0040 - 004F	0.3K	BIOS Data Area
0050 - 006F	0.5K	System Data
0070 - 0436	15K	DOS
0437 - 0600	7.2K	Program Area
0601 - 9F7F	613K	[Available]
= Conventional memory ends at 638K =		
A000 - AFFF	64K	VGA Graphics
B000 - B7FF	32K	Unused
B800 - B7FF	32K	VGA Text
C000 - CE7F	55K	Video ROM
CE80 - DFFF	71K	Unused
E000 - EFFF	64K	System ROM
F000 - FFFF	64K	System ROM
HMA	64K	First 64K Extended

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	SMARTDRV	System Timer
IRQ 1	SMARTDRV	Keyboard Event
IRQ 2	[Unassigned]	Usable IRQ
IRQ 3	System ROM	COM 2
IRQ 4	System ROM	COM 1
IRQ 5	[Unassigned]	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	[Unassigned]	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	[Unassigned]	Usable IRQ
IRQ 10	[Unassigned]	Usable IRQ
IRQ 11	[Unassigned]	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	[Unassigned]	Usable IRQ

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support your products, projects and business.



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