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User's Manual

Single Board Computer 3307850

Version 1.0, December 2008

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your 3307850 system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory to get a safe installation and provides a programming guide of Watch Dog Timer function.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Global American Inc.** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.globalamericaninc.com.

Chapter 1
System Overview

1.1 Introduction

3307850, the PICMG 1.3 SHB (Single Host Board) combined with either the Intel® Core 2 Duo processor, and with support next-generation 45nm Intel® Core 2 processor family. The attractive Core 2 Duo processor does not only posses amazing parallel computing power but also generates 65W TDP (Thermal Design Power). That makes the system more powerful and reliable with dual-core processor with smaller and quieter cooling fan.

The SHB adopted Intel® Q35 & ICH9DO chipset. The Q35 embedded Graphics Media Adapter 3100 is the 4th generation Intel integrated graphics controller that supports DirectX 9.0, Shader model 2.0, 256MB of video memory. More than that, user could utilize even higher-end, the latest PCI Express x16 interface graphics card via backplane.

To meet bandwidth of storage and expansion cards requirement, the 3307850 was designed flexible with four PCI Express lanes via backplane. Those four PCI Express lanes could be four PCI Express x1 links or one PCI Express x4 link. Four PCI Express x1 links configuration can support more PCI Express x1 devices via backplane and one PCI Express x4 link configuration can support RAID card or special add-on cards such as image processing board. In addition, the flexible configuration can be leveraged with bridge on backplane to support more PCI or PCI-X slots that benefits industries with legacy support.

Advanced Management Technology (AMT) is feature that 3307850 equipped. This technology provides remote access capability via Intel® Gigabit Ethernet controller. The new technology is a hardware-based solution that uses out-of-band communication for system management access to client systems. Beside that, the hardware and software information can be gathering by 3rd party software then storage in SPI interface EEPROM. Therefore, asset management could be done at the same time.

Six Serial ATA channels support via ICH9DO, connecting one device per channel. One channel is configured as an external Serial ATA (eSATA) channel. eSATA is alternative solution of external interface. This function can communicate with multiple drives via port multiplier.

3307850 features:

- Support Intel® Core 2 Duo, Celeron 440 processor in an LGA775 socket with 1333/1066/800MHz Front Side Bus
- Dual 240-pin DDR2 SDRAM DIMM socket, support for DDR2 800/667 DIMMs, up to 4GB system memory
- Intel® Q35 integrated GMA 3100 that supports MPEG-2 Decode, DirectX 9.0c, OpenGL 1.4 and Shader Model 2
- Equipped dual Intel Gigabit Ethernet ports
- One PCI Express x16 external expansion, one PCI Express x4 link (can be configured as four PCI Express x1) and four PCI devices via backplane

The PICMG 1.3 SHB is the best solution of applications such like flight simulation, image processing, broadcasting and so on that need performance of display and storage.

1.2 Check List

The 3307850 package should cover the following basic items:

- ✓ One 3307850 single host board
- ✓ One dual Serial ports cable kit
- ✓ One single Parallel port cable kit
- ✓ One FDD cable
- ✓ Two 7-pin SATA signal cables
- ✓ One Installation Resources CD-Title

Optional: One bracket with PS/2 keyboard and mouse

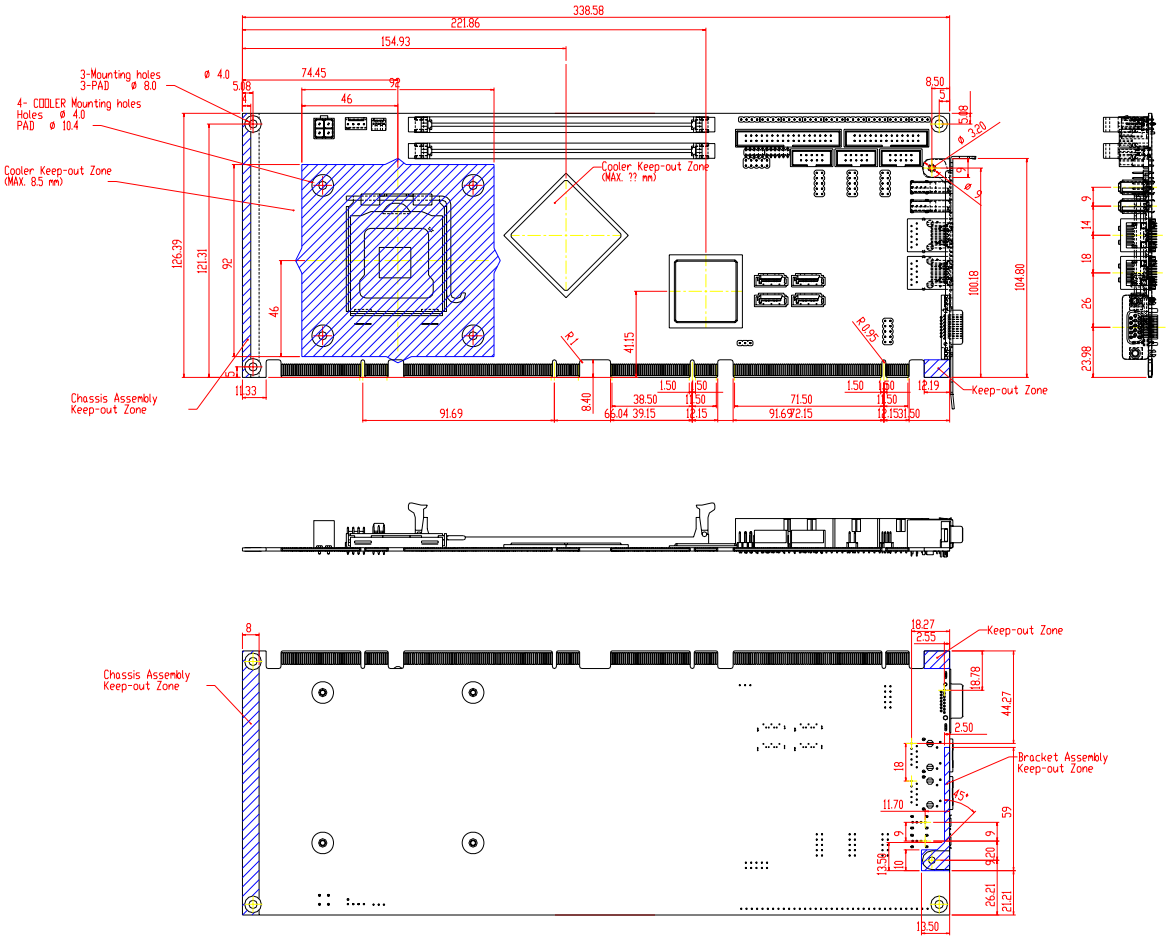
If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**
  - Intel® Core 2 Duo/Celeron 440 Processor
  - FSB: 1,333/1066/800MHz
- **BIOS**
  AMI system BIOS with SPI Serial CMOS EEPROM with easy upgrade function ACPI, DMI, Green function and Plug and Play Compatible
- **Main Memory**
  - Support dual-channel DDR2 memory interface
  - Non-ECC, non-buffered DIMMs only
  - Two DIMM sockets support 800/667 DDR2-SDRAM up to 4GB System Memory
- **L2 Cache Memory**
  Built-in Processor
- **Chipset**
  Intel® Q35 GMCH and ICH9DO chipset
- **Bus Interface**
  - Follow PICMG 1.3 Rev 1.0 standard (PCI Express and PCI)
  - Support four PCI Express x1 (can be aggregated as one PCI Express x4) through backplane
  - Support four PCI devices through backplane
- **SATA**
  - Four SATA 300 ports on-board and dual SATA 300 ports via backplane
  - Support Intel® Matrix Storage Technology based on Intel® ICH9DO
- **Floppy Drive Interface**
  Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD
- **Serial Ports**
  Support two high-speed 16C550 compatible UARTs with 16-byte T/R FIFOs
- **Parallel Port**
  Support one parallel port with SPP, EPP and ECP modes
- **USB Interface**
  Support twelve USB (Universal Serial Bus) ports (two USB ports on bracket that dedicated to keyboard & mouse; six USB ports on-board and four USB ports via backplane) for high-speed I/O peripheral devices
- **PS/2 Mouse and Keyboard Interface**
  Support one 10-pin connector for external PS/2 keyboard/mouse connection
- **Auxiliary I/O Interfaces**
  System reset switch, external speaker, Keyboard lock and HDD active LED, etc

- **Real Time Clock/Calendar (RTC)**
  Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention
- **Watchdog Timer**
  - Support WDT function through software programming for enable/disable and interval setting
  - Generate system reset
- **On-board VGA**
  GMCH integrated graphics, 400MHz core frequency; share system memory up to 64MB for system with greater than or equal to 192MB of system memory
- **On-board Ethernet LAN**
  Dual Intel® PCI Express x1 interface based Gigabit Ethernet to support RJ-45 connector
- **High Driving GPIO**
  Support 8 programmable high driving GPIO
- **Cooling Fans**
  Support one 4-pin power connector for CPU fan and one 3-pin power connector for system fan
- **System Monitoring Feature**
  Monitor CPU temperature, system temperature and major power sources, etc.
- **Bracket**
  Support dual Ethernet port with 2 indicators, dual USB ports and one CRT port
- **Outline Dimension (L X W):**
  338.5mm (13.33") X 122mm (4.8")
- **Power Requirements:**
  - +12V@ 5.4A
  - +5V @ 5.0A
  - Test configuration:
    - CPU: Intel® Core 2 Duo 2.13GHz(FSB: 1,066 / L2 cache: 2MB)
    - Memory: Transcend (TS128MLQ64V6J-E) 1GB 667MHZ X2
    - Primary Master SATA HDD: Seagate ST380817AS 80G
    - OS: Microsoft Windows 2000 Professional
    - Test Programs: BurnIn Test V4.0
    - Run Time: Full loading
- **Operating Temperature:**
  0°C ~ 60°C (23°F ~ 140°F)
- **Storage Temperature:**
  -20°C ~ 80°C
- **Relative Humidity:**
  5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing

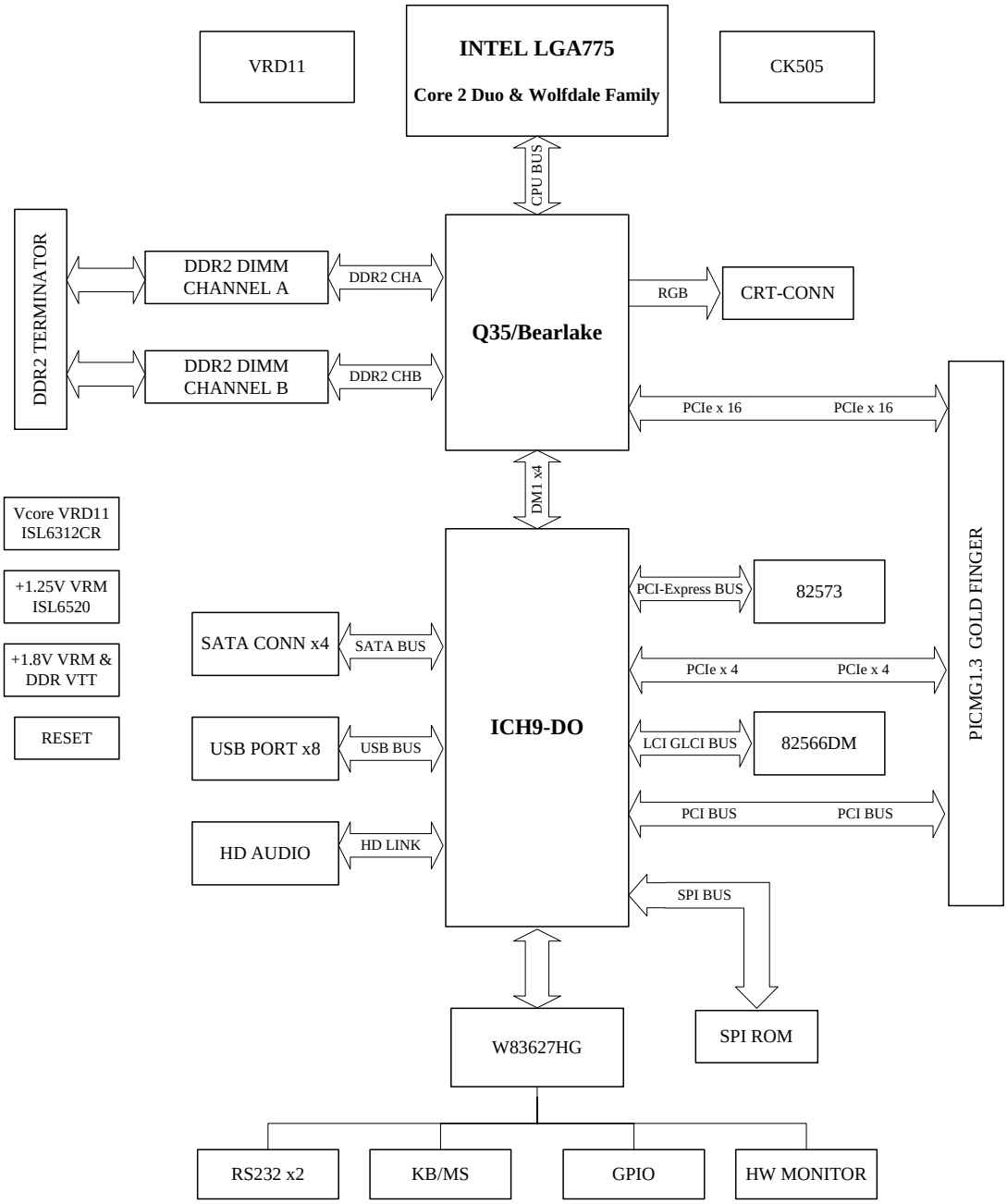


1.4 System Architecture

3307850 adopts Intel® Q35 Express chipset that supports Intel® Core 2 Duo processor that based on Intel innovative Core Mircoarchitecture Technology. Q35 GMCH (Graphics Memory Controller Hub) embedded Graphics Media Accelerator 3100 (GMA 3100) and features PCI Express x16 graphics interface via backplane that supports the latest high-performance graphics cards. Along with the highest 1,333MHz FSB of processor, the parallel system memory is up to DDR2 800 as well.

The companion I/O controller, ICH9DO has six PCI Express x1 links that throughput is 2.5Gbps per direction. And they were designed as interface of dual Gigabit Ethernet ports on-board and four PCI Express x1 expansion via backplane. One special characteristic of the ICH9DO is the capability to aggregate these four PCI Express x1 link as one PCI Express x4 link. And that is what user can benefit for PCI Express x4, high throughput storage expansion card via backplane.

ICH9DO provides six SATA 300 ports, together with Intel® Matrix Storage Technology (MST), the 3307850 offers cost effective RAID 0, 1, 5 and 10
that seamlessly protects against data loss from hard drive failure. It also support external SATA (eSATA) function that can communicate with multiple drives via port multiplier. Dual SATA ports and four USB ports are routed to gold finger for better wiring consideration of these two kinds of interface via backplane. Super I/O chip, W83627 is responsible for PS/2 keyboard/mouse, UARTs, FDC, hardware monitor, Parallel, and Watch Dog Timer interface.



3307850 System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on 3307850 are in the proper position. The default settings shipped from factory are marked with an asterisk (★).

2.1 Jumper Setting

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".

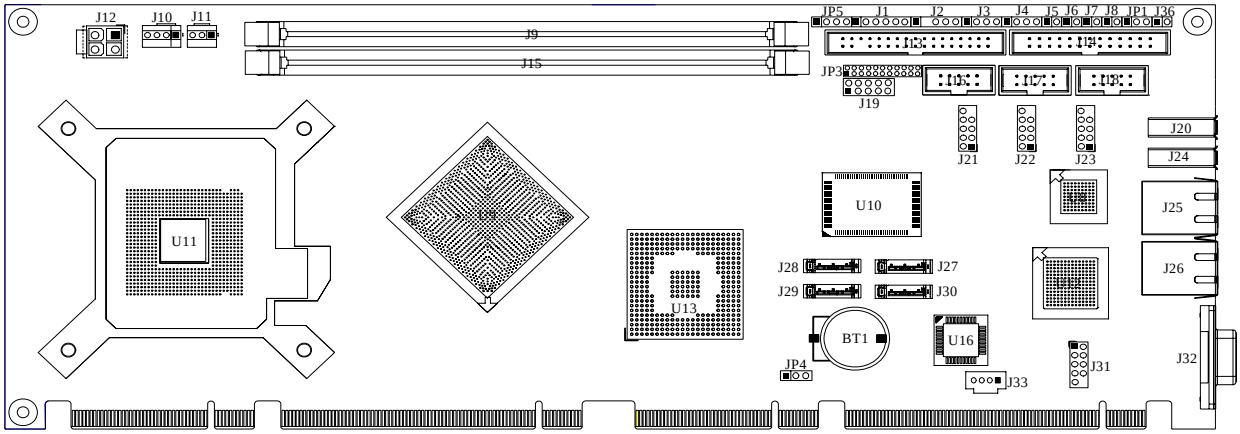


Figure 2-1 3307850 Jumper Location

JP4 : CMOS Clear

JP4	Function
1-2 Short	Normal Operation
2-3 Short	Clear CMOS Contents

JP3 : COM2 (J17) Interface Selection

JP3	Function
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

JP1 : Intel 82573L Interface Selection

Reserve for Enable or disable LAN function.
Normal control at 1-2 short.

JP5 : PCI-E X1,X4 Interface Selection

JP5	Function
Short (1-2 , 3-4)	PCI-E X4 (Support one slot)
Open	PCI-E X1 (Support four slot)

2.2 Connector Allocation

I/O peripheral devices and Flash disk will be connected to these interface connectors.

Connector Function List

Connector	Description	Remark
J1	IrDA Connector	6x1 pin header
J2	SMBUS Connector	5x1 pin header
J3	External Speaker Connector	4x1 pin header
J4	Gigabit Ethernet Indication (ACT/LINK) Header	4x1 pin header
J5	Power On/Off Header (AT MODE)	Optional
J6	SATA LED	
J7	MEM LED	
J8	Suspend LED	
J10	FAN 1 (CPU FAN) Power Connector	
J11	FAN 2 (SYSTEN FAN) Power Connector	
J12	+12V Power Connector	
J13	Floppy Connector	
J14	Parallel Port Connector	
J16	COM1 Serial Port 1 Connector	
J17	COM2 Serial Port 2 Connector	
J18	External PS/2 Keyboard/Mouse Connector	
J19	General Purpose I/O Connector	
J20	Internal USB Connector	
J21	External USB Connector	
J22	External USB Connector	
J23	External USB Connector	
J24	Internal USB Connector	

J25	Ethernet RJ-45 Connector (LAN 1) 82566DM	
J26	Ethernet RJ-45 Connector (LAN 2) 82573L	
J27	SATA 1 Connector	
J28	SATA 0 Connector	
J29	SATA 3 Connector	
J30	SATA 2 Connector	
J31	Audio Connector	
J32	VGA D-SUB Connector	
J33	Audio CD -IN Connector	
J36	CASEOPEN#	Optional

Pin Assignments of Connectors

J1 : IrDA Connector

PIN No.	Signal Description
1	+5V
2	N/C
3	IRRX
4	IRTX
5	Ground
6	N/C

J2 : SMBUS Connector

PIN No.	Signal Description
1	SMB_CLK
2	N/C
3	Ground
4	SMB_DAT
5	+5V

J3 : External Speaker Connector

PIN No.	Signal Description
1	Speaker Signal Output (Open-drain w/ internal series 33 Ohm)
2	N/C
3	Ground
4	+5V

J4 : Gigabit Ethernet LAN Indication (ACT/LINK) Header

PIN No.	Signal Description
1	82566DM ACT
2	82566DM LINK
3	82573L ACT/LINK
4	+3.3V

J6 : HDD Active LED Connector

PIN No.	Signal Description
1	SATALED#
2	+3.3V

J7 : AMT Active LED Connector

PIN No.	Signal Description
1	AMTLED
2	+5.5V

J8 : Suspend Active LED Connector

PIN No.	Signal Description
1	Suspend
2	+5.5V

J10 : CPU Fan Connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Control
4	Fan Speed Detecting signal

J11 : System Fan Connector

PIN No.	Signal Description
1	Ground
2	+12V
3	Fan Speed Detecting signal

J12 : +12V POWER Connector

PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

J13 : Floppy Interface

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select
3	Ground	4	N/C
5	Ground	6	DRVEN1
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor ENB#
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Head Select#
33	Ground	34	Disk Change#

J14 : Parallel Port Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	14	Auto Form Feed#
2	Data0	15	Error#
3	Data1	16	Initialization#
4	Data2	17	Printer Select IN#
5	Data3	18	Ground
6	Data4	19	Ground
7	Data5	20	Ground
8	Data6	21	Ground
9	Data7	22	Ground
10	Acknowledge#	23	Ground
11	Busy	24	Ground
12	Paper Empty	25	Ground
13	Printer Select	26	NC

J16 : COM1 Serial Port

PIN No.	Signal Description
1	DCD
2	DSR
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR
8	RI
9	Ground
10	N/C

J17 : COM2 Serial Port 2 Connector

PIN No.	Signal Description		
	RS-232	**RS-422**	**RS-485**
1	DCD (Data Carrier Detect)	TX-	DATA-
2	RXD (Receive Data)	TX+	DATA+
3	TXD (Transmit Data)	RX+	N/C
4	DTR (Data Terminal Ready)	RX-	N/C
5	GND (Ground)	GND	GND
6	DSR (Data Set Ready)	N/C	N/C
7	RTS (Request to Send)	N/C	N/C
8	CTS (Clear to Send)	N/C	N/C
9	RI (Ring Indicator)	N/C	N/C
10	N/C	N/C	N/C

Note:
J17 (COM2) could be configurable as RS-232/422/485 with jumper JP3.

J18 : External PS/2 Keyboard/Mouse Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Mouse Clock

J19 : General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

Note:
All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each Fan.

J21/J22/J23 : External USB Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground
	Key(no pin)	10	N/C

Note:
5V Dual is always available. It's supplied by either 5V VCC power source in normal operation mode or 5V standby power source in standby mode.

J31 : Audio MIC/Line-in/Line-out Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	MIC with Reference Voltage	2	Analog Ground
3	Line-in Left Channel	4	Analog Ground
5	Line-in Right Channel	6	Analog Ground
7	Line-out Left Channel	8	Analog Ground
9	Line-out Right Channel	10	N/C

J32 : On-board VGA Connector

PIN No.	Signal Description
1	Red
2	Green
3	Blue
4	Monitor ID0 (MONID0) (5V I/F)
5	Ground
6	Ground
7	Ground
8	Ground
9	+5V
10	Ground
11	Monitor ID1 (MONID1) (5V I/F)
12	VGA DDC Data (5V I/F)
13	Horizontal Sync. (HSYNC) (5V I/F)
14	Vertical Sync. (VSYNC) (5V I/F)
15	VGA DDC Clock (5V I/F)

J33 : Audio CD-IN Connector

PIN No.	Signal Description
1	CD-in Left Channel
2	CD Ground
3	CD Ground
4	CD-in Right Channel

Chapter 3
System Installation

Chapter 3 instructs you to set up system; the additional information is enclosed to help you set up onboard PCI device and handle WDT operation in software programming.

3.1 Intel® LGA 775 Processor

Installing LGA 775 CPU

1) Lift the handling lever of CPU socket outwards and upwards to the other end. Following step A position to step B position (Figure 3-1).

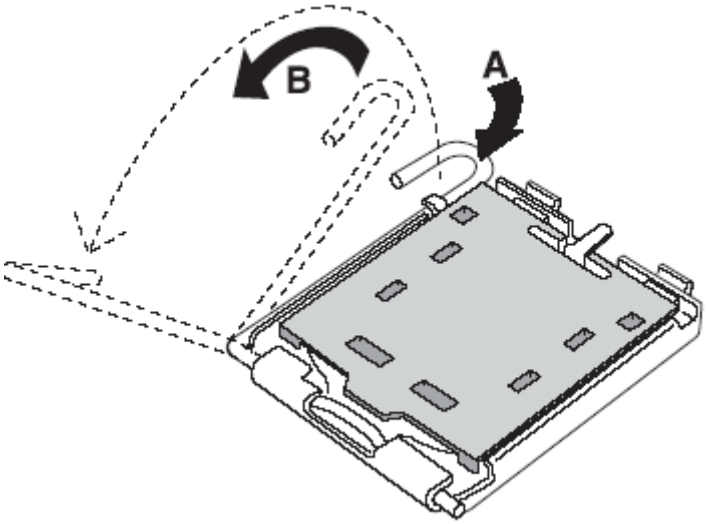


Figure 3-1

2) Align the processor pins with pinholes on the socket. Make sure that the notched corner or dot mark (pin 1) of the CPU corresponds to the socket's bevel end. Then press the CPU gently until it fits into place (see Fig.3-4). If this operation is not easy or smooth, don't do it forcibly. You need to check and rebuild the CPU pin uniformly.

Triangle mark is meaning first pin position; kindly assemble and take aim at notch of top and bottom between CPU and socket.

Figure 3-2

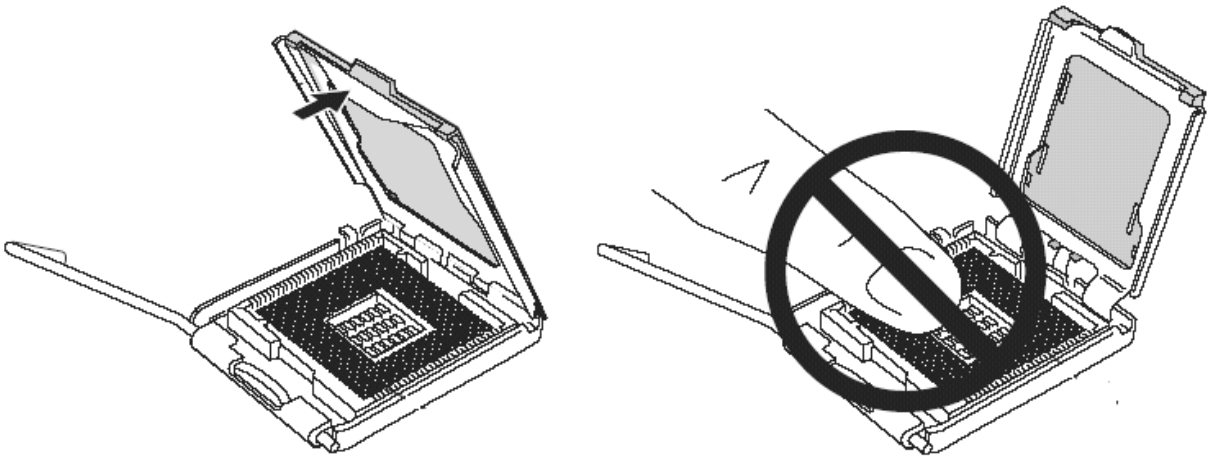


Figure 3-3

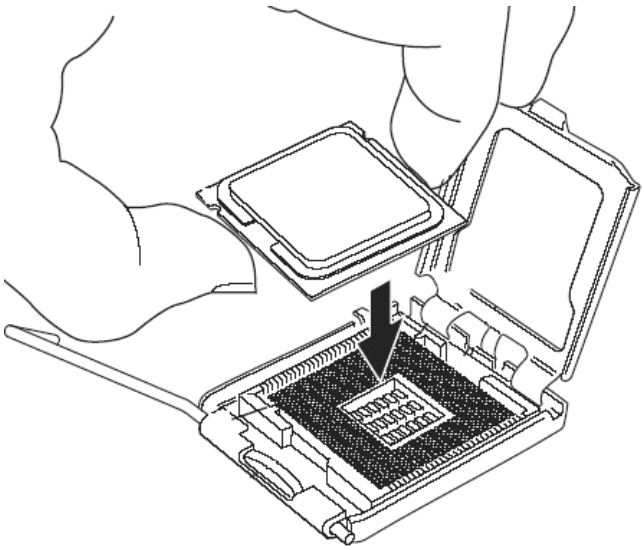


Figure 3-4

Precaution! (See fig.3-3) Don't touch directly by your hand or impacts internal align balls of CPU socket to avoid motherboard destruction, it is a precise actuator.

3) Push down the lever to lock processor chip into the socket once CPU fits.

4) Follow the installation guide of cooling fan or heat sink to mount it on CPU surface and lock it on the LGA 775 package.

5) You should know LGA 775 processor need extra 12V power source.
Don't forget to connect 4pin (0r 8 pin) 12V connector to J12!

J12 : 12V CPU Supplementary Connector

PIN No.	Signal Description
1	Ground
2	Ground
3	+12V
4	+12V

Removing CPU

1) Unlock the cooling fan first.
2) Lift the lever of CPU socket outwards and upwards to the other end.
3) Carefully lifts up the existing CPU to remove it from the socket.
4) Follow the steps of installing a CPU to change to another one or place handling bar to close the opened socket.

CPU Application

Supports Intel® Core 2 Duo, Celeron® 440 ,Wolfdale M, Wolfdale L processor in an LGA775 socket equipped with dual core, Hyper-Threading, EM64T, EIST, and XD & VT technologies.

3.2 Main Memory

3307850 provides 2 x 240-pin DDR2-SDRAM DIMM sockets support 1.8V dual-channel DDR2 800/667 non-ECC DIMMs. The maximum memory size can be up to 8GB. Auto detecting memory clock is according to BIOS CMOS settings.

For system compatibility and stability, don't use memory module without brand. You can also use single-sided or double-sided DIMM in both slots.

Watch out the contact and lock integrity of memory module with socket, it will impact on the system reliability. Follow normal procedures to install your DRAM module into memory socket. Before locking, make sure that all modules have been fully inserted into the card slots.

Dual Channel DDR2 DIMMs

Dual Channel DDR2 memory technology doubles the bandwidth of memory bus. Adequate or higher bandwidth of memory than processor would increase system performance. To enable Dual Channel DDR2 memory technology, you have to install dual identical memory modules in both memory sockets. Following tables show bandwidth information of different processor and memory configurations.

Memory Frequency	Dual Channel DDR Bandwidth	Single Channel DDR Bandwidth
800MHz	25.6 GB/s	12.8 GB/s
667 MHz	21.2 GB/s	10.6 GB/s

Note:
To maintain system stability, don't change any of DRAM parameters in BIOS setup to upgrade your system performance without acquiring technical information.

CPU FSB / Memory Frequency synchronization

Support different memory frequencies depending on the CPU front side bus and the type of DDR2 DIMM. Watch Out, it's meaning that memory maximum frequency on configuration, which is synchronization and based on CPU FSB.

CPU FSB	Memory Frequency
1066MHz	533 / 667 / 800MHz
800 MHz	533 / 667 / 800MHz

3.3 Installing the Single Board Computer

To install your 3307850 into standard chassis or proprietary environment, you need to perform the following:

Step 1: Check all jumpers setting on proper position.
Step 2: Install and configure CPU and memory module on right position.
Step 3: Place 3307850 into the dedicated position in your system.
Step 4: Attach cables to existing peripheral devices and secure it.

WARNING

Bus Interface Fully complies with PCI Local Bus specification V2.2 (support 2 master PCI slots); and Please follow section 3.31 to 3.3.5 instruction to install hardware dricer.

3.3.1 Chipset Component Driver

The chipset on 3307850 is a new chipset that a few old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows 2000 /XP / Server 2003, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in 3307850 CD-title.

3.3.2 Intel Integrated Graphics GMCH Chip

Using GMCH High performance graphic integrated chipset (Intel GMA 3000) is aimed to gain an outstanding graphic performance. Shared 128 accompany it to 256MB/Maximum system DDR2-SDRAM with Total Graphics Memory. This combination makes 3307850 an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting BIOS of "Advanced Chipset Feature" and set "PEG/Onchip VGA Control" to [PEG Port] (please kindly refer section 4.6 of chapter 4 configuration), and then the add-on PCI or PCI Express by 16 VGA Card can take over the system display.

Drivers Support

Please find hardware driver of 82965 GMCH in the 3307850 CD-title. Drivers support Windows 2000 / XP System 32-bit & Windows XP System 64-bit.

Windows 2000/XP (32bit): Please execute Install for Windows 2000/XP System 32-Bit file to start graphics driver installation.

Windows XP (64-bit): Please execute Install for Windows XP System 64-bit file to start graphics driver installation.

3.3.3 On-board Fast Ethernet Controller

Drivers Support

Please find Ethernet combination driver for operating Intel 82573L and 82566DM Gigabit LAN from 3307850 CD-title. The drivers support Windows 2000/XP System 32-Bit & Windows XP System 64-bit.

Windows 2000/XP (32bit): Please execute Install for Windows 2000/XP System 32-Bit file to start Intel LAN driver installation.

Windows XP (64-bit): Please execute Install for Windows XP System 64-bit file to "Ethernet\intel\intel_Gigabit_64bit\"; Pass below button into the dictionary.

LED Indicator (for LAN status)

3307850 provides three LED indicators to report Intel 82566DM Gigabit Ethernet interfaces status. Please refer to the table below as a quick reference guide.

<table>
<tr><th rowspan="2">82566DM</th><th rowspan="2">Color</th><th rowspan="2">Name of LED</th><th colspan="3">Operation of Ethernet Port</th></tr>
<tr><td>Linked</td><td colspan="2">Active</td></tr>
<tr><td>Status LED</td><td>Yellow</td><td>LAN Linked & Active LED</td><td>On</td><td colspan="2">Blinking</td></tr>
<tr><td rowspan="2">Speed LED</td><td>Orange</td><td rowspan="2">LAN speed LED</td><td>Giga Mbps</td><td>100 Mbps</td><td>10 Mbps</td></tr>
<tr><td>Green</td><td>Orange</td><td>Green</td><td>Off</td></tr>
</table>

3.3.4 On-board AC-97 Audio Device

Please find Realtek ALC260 Audio driver of 3307850 CD-title. The drivers support Windows 2000/XP/Server 2003.

3.3.5 Intel Matrix Storage Manager Device

Drivers Support

Please find utility tool for Intel ICH9DO of 3307850 CD-title. The drivers support Windows 2000/XP System 32-Bit & Windows XP System 64-bit.

Installing Serial ATA hard disks

The 3307850 supports Six Serial ATA hard disk drives. For optimal performance, install identical drives of the same model and capacity when creating a disk array.

To install the SATA hard disks for a RAID configuration:

1. Install the SATA hard disks into the drive bays.
2. Connect the SATA signal cables.
3. Connect a SATA power cable to the power connector on each drive.

Intel RAID configurations

This 3307850 supports RAID 0, RAID 1, RAID 5, RAID (0+1) and Intel® Matrix Storage configurations for Serial ATA hard disks drives through the Intel ICH9DO Southbridge chip.

RAID configurations

RAID 0 (Data striping) optimizes two identical hard disk drives to read and write data in parallel, interleaved stacks. Two hard disks perform the same work as a single drive but at a sustained data transfer rate, double that of a single disk alone, thus improving data access and storage. Use of two new identical hard disk drives is required for this setup.

RAID 1 (Data mirroring) copies and maintains an identical image of data from one drive to a second drive. If one drive fails, the disk array management software directs all applications to the surviving drive as it contains a complete copy of the data in the other drive. This RAID configuration provides data protection and increases fault tolerance to the entire system. Use two new drives or use an existing drive and a new drive for this setup. The new drive must be of the same size or larger than the existing drive.

RAID 10 is data striping and data mirroring combined without parity (redundancy data) having to be calculated and written. With the RAID 10 configuration you get all the benefits of both RAID 0 and RAID 1 configurations. Use four new hard disk drives or use an existing drive and three new drives for this setup.

RAID 5 stripes both data and parity information across three or more hard disk drives. Among the advantages of RAID 5 configuration include better HDD performance, fault tolerance, and higher storage capacity. The RAID 5 configuration is best suited for transaction processing, relational database applications, enterprise resource planning, and other business systems. Use a minimum of three identical hard disk drives for this setup.

Intel Matrix Storage Manager. The Intel® Matrix Storage technology supported by the ICH9DO chip allows you to create a RAID 0 and a RAID 1 set using only two identical hard disk drives. The Intel® Matrix Storage technology creates two partitions on each hard disk drive to create a virtual RAID 0 and RAID 1 sets. This technology also allows you to change the hard disk drive partition size without losing any data.

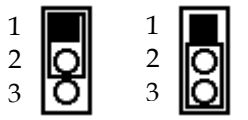
3.3.6 AMT Function Installation

A major barrier to greater IT efficiency has been removed by Intel® Active Management Technology (Intel® AMT) a feature on Intel® vPro™ technology. Using built-in platform capabilities and popular third-party management and security applications, Intel AMT allows IT to better Discover, Heal, and Protect their networked computing assets.

Installing ME (Management Engine) Drivers (which includes HECI Driver and LMS_SOL Driver) and operating PCI serial port and PCI simple communications controller.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable CMOS Clear Function hardware circuit by putting jumpers at proper position.



Normal Clear

JP4	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS contents

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

3307850 allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to Winbond W83627HG-AW data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)

Below are some example codes, which demonstrate the use of WDT.

```
//Step1. Enter W83627HG configuration registers mode:
outportb(0x2E, 0x87);
outportb(0x2E, 0x87);

//* Step2. Pin89 to be WDTO
outportb(0x2E, 0x2b);
outportb(0x2E + 1, 0x04);

//* Step3. Select logic device 8:
outportb(0x2E, 0x07);
outportb(0x2E + 1, 0x08);
```

```
//* Step4. Config WDT using second to be unit:
outportb(0x2E, 0xf5);
outportb(0x2E + 1, 0x00);

//* Step5. Set WDT time-out time:
outportb(0x2E, 0xf6);
outportb(0x2E + 1, time_out);

//* Step6. Exit configuration registers mode:
outportb(0x2E, 0xaa);
```

3.6 GPIO

The 3307850 provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.5.1 Pin assignment

J19: General Purpose I/O Connector

PIN No.	Signal Description
1	General Purpose I/O Port 0 (GPIO0)
2	General Purpose I/O Port 1 (GPIO1)
3	General Purpose I/O Port 2 (GPIO2)
4	General Purpose I/O Port 3 (GPIO3)
5	Ground
6	General Purpose I/O Port 4 (GPIO4)
7	General Purpose I/O Port 5 (GPIO5)
8	General Purpose I/O Port 6 (GPIO6)
9	General Purpose I/O Port 7 (GPIO7)
10	+5V

All General Purpose I/O ports can only apply to standard TTL ± 5% signal level (0V/5V), and each source sink capacity up to 12mA.

3.5.2 3307850 GPIO Programming Guide

There are 8 GPIO pins on 3307850. These GPIO pins are from SUPER I/O (W83627GH-AW) GPIO pins, and can be programmed as Input or Output direction.

J15 pin header is for 8 GPIO pins and its pin assignment as following :

J19_Pin1=GPIO0:from SUPER I/O_GPIO10 with Ext. 4.7K PH
J19_Pin2=GPIO1:from SUPER I/O_GPIO11 with Ext. 4.7K PH
J19_Pin3=GPIO2:from SUPER I/O_GPIO12 with Ext. 4.7K PH
J19_Pin4=GPIO3:from SUPER I/O_GPIO13 with Ext. 4.7K PH
J19_Pin6=GPIO4:from SUPER I/O_GPIO14 with Ext. 4.7K PH
J19_Pin7=GPIO5:from SUPER I/O_GPIO15 with Ext. 4.7K PH
J19_Pin8=GPIO6:from SUPER I/O_GPIO16 with Ext. 4.7K PH
J19_Pin9=GPIO7:from SUPER I/O_GPIO17 with Ext. 4.7K PH
<<<<< Be careful Pin5=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of W83627HG-AW needed to be programmed to control the GPIO direction, and status(GPI)/value(GPO). CR00h ~ CR2F are common (global) registers to all Logical Devices (LD) in W83627HG. CR07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO10~17 registers.

Programming Guide:

Step1: CR2A_Bit [7.2]. P [1,1,1,1,1,1]; to select multiplexed pins as GPIO10~17 pins
Step2: LD7_CR07h.P [07h]; Point to LD7
Step3: LD7_CR30h_Bit0.P1; Enable LD7
Step4: Select GPIO direction, Get Status or output value.

LD7_CRF0h; GPIO17 ~ 10 direction, 1 = input, 0 = output pin
LD7_CRF2h.P [00h]; Let CRF1 (GPIO data port) non-invert to prevent from confusion
LD7_CRF1h; GPIO17~10 data port, for input pin, get status from the related bit, for output pin, write value to the related bit.

For example,

LD7_CRF0h_Bit4.P0; Let GPIO14 as output pin
LD7_CRF2h_Bit4.P0; Let CRF1_Bit4 non-inverted
LD7_CRF1h_Bit4.P0; Output "0" to GPIO14 pin (J25_Pin6)

LD7_CRF0h_Bit0.P1; Let GPIO10 as input pin
LD7_CRF2h_Bit0.P0; Let CRF1_Bit0 non-inverted
Read LD7_CRF1h_Bit0; Read the status from GPIO10 pin (J25_Pin1)

How to access W83627HG CR?

In 3307850, the EFER = 002Eh, and EFDR = 002Fh.
EFER and EFDR are 2 IO ports needed to access W83627HG-AW CR.
EFER is the Index Port, EFDR is the Data Port.
CR index number needs to be written into EFER first,
Then the data will be read/written from/to EFDR.

To R/W W83627HG-AW CR, it is needed to Enter/Enable Configuration Mode first. When completing the programming, it is suggested to Exit/Disable Configuration Mode.

Enter Configuration Mode: Write 87h to IO port EFER twice.
Exit Configuration Mode: Write AAh to IO port EFER.

3.5.3 Example

```
void enter_Superio2_CFG(void)
{
      outportb(0x2E, 0x87);
      outportb(0x2E, 0x87);
}


void exit_Superio2_CFG(void)
{
      outportb(0x2E, 0xAA);
}


void Set_CFG2(unsigned char Addr2,unsigned char Value2)
{
   unsigned char d2;
      outportb(0x2E, Addr2);
      delay(2);
      outportb(0x2E +1, Value2);
      delay(2);
}
```

```
unsigned char Get_CFG2(unsigned char Addr2)
{
   unsigned char d2;
      outportb(0x2E, Addr2);
      delay(2);
      d2 = inportb(0x2E +1);
      delay(2);
      return(d2);
}

int main(void)
{

      unsigned char d2;

      enter_Superio2_CFG();
      /* CR2A B7 = 1 selet GPIO Port 1*/
      d2 = Get_CFG2(0x2A);
      d2 = (d2 & 0x7F) | 0x80;
      Set_CFG2(0x2A, d2);

      /* IO test loop 1 */
      /* Set GPIO Port 1 of Superio 2 Enable */

      Set_CFG2(0x07, 0x07);        /* Select logic device 07 of Superio2*/
      Set_CFG2(0x30, 0x01);        /* Enable GPIO Port 1 of Superio2*/



      /* IO test loop 1 */

      /* Set GPIO Port 1 of Superio2 Enable */
      Set_CFG2(0x07, 0x07);        /* Select logic device 07*/
      Set_CFG2(0xF0, 0x0F);       /* GPIO Port 1 of Superio2 is [ooooiiii], o: output,
i:input */
      Set_CFG2(0xF2, 0x00);       /* GPIO Port 1 of Superio2 is non-inversed*/
```

```
Set_CFG2(0x07, 0x07);       /* Select logic device 07*/
Set_CFG2(0xF1, 0xFF);       /* Initial back all GPIO Port1 of Superio 2 to hi */

Set_CFG2(0x07, 0x07);       /* Select logic device 07*/
Set_CFG2(0xF1, 0xEF);       /* GP14 of Superio2 -> ~GP10 of Superio2 */
Set_CFG2(0x07, 0x07);       /* Select logic device 07 of Superio2*/
d2 = Get_CFG2(0xF1);        /* get GPIO Port 2 data */

if (d2 == 0xEE )

   printf("\n GPIO14->10 test ok");
else
   printf("\n GPIO14->10 test fail ");
```

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Device Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0700-0483	16K	DOS
0484-053F	2.9K	Program Area
0540-9EFE	614K	[Available]
9EFE-9EFE	0.1K	Unused
= Conventional memory ends at 640K =		
9F00-9FBF	3K	Extended BIOS Area
9FC0-9FFF	1K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CAFF	44K	Video ROM
CB00-CC49	5.2K	Unused
CC4A-CFFF	14K	High RAM
D000-DFFF	64K	Page Frame
E000-EEFF	60K	Unused
EF00-EFFF	4K	ROM
F000-FFFF	64K	System ROM
HMA	64K	First 64K Extended

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	Unassigned	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	Unassigned	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	Unassigned	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	Unassigned	Usable IRQ
IRQ 10	Unassigned	Usable IRQ
IRQ 11	Unassigned	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	Unassigned	Usable IRQ

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support your products, projects and business.

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