integration with integrity

3308220 User's Manual

3.5" Embedded Controller

Version V1.1

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Safety Instructions

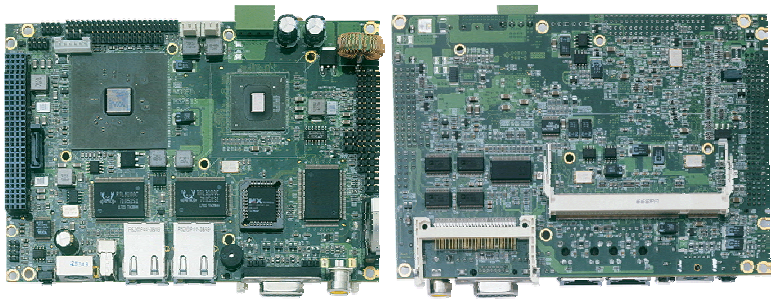
Integrated circuits on computer boards are sensitive to static electricity. To avoid damaging chips from electrostatic discharge, observe the following precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before handling a board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. This helps to discharge any static electricity on your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components. Fasten the ALLIGATOR clip of the strap to the end of the shielded wire lead from a grounded object. Please wear and connect the strap before handle the 3308220 to ensure harmlessly discharge any static electricity through the strap.
- Please use an anti-static pad when putting down any components or parts or tools outside the computer. You may also use an anti-static bag instead of the pad. Please inquire from your local supplier for additional assistance in finding the necessary anti-static gadgets.

NOTE: *DO NOT TOUCH THE BOARD OR ANY OTHER SENSITIVE COMPONENTS WITHOUT ALL NECESSARY ANTI-STATIC PROTECTIONS.*

Chapter 1

General Description



The 3308220 is a VIA CX700 chipset-based board designed. The 3308220 is an ideal all-in-one embedded engine board. Additional features include an enhanced I/O with CF, CRT/LVDS, TV-Out, dual LAN, audio, SATA, 4 COM, USB2.0, and PC/104 Plus interfaces.

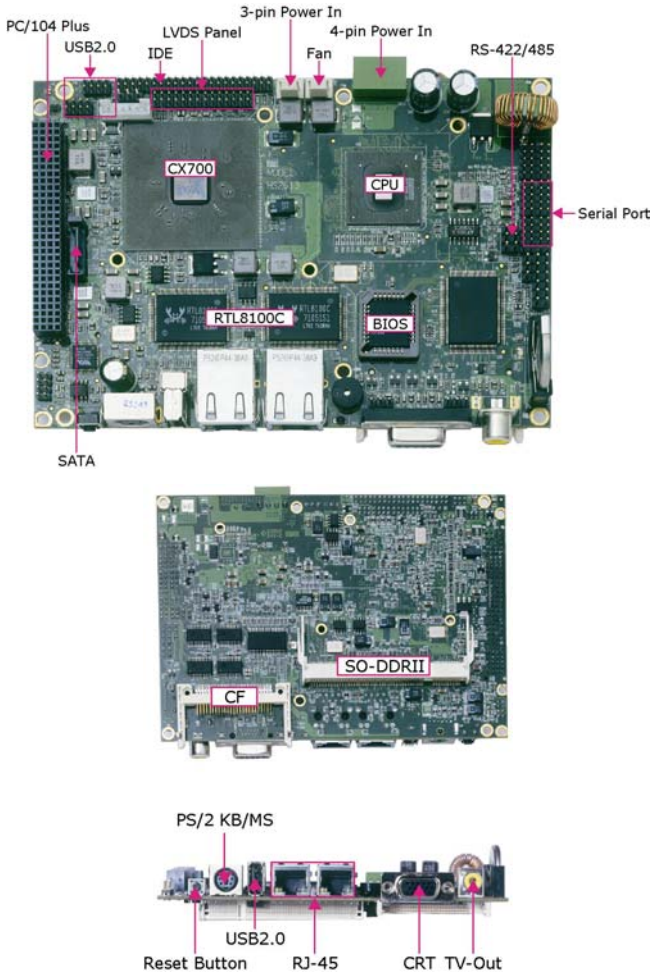
Its onboard ATA/33/66/100 to IDE drive interface architecture allows the 3308220 to support data transfers of 33 or 66MB/sec. to one IDE drive connection. Designed with the VIA CX700, the board supports VIA C7 or ULV VIA V4 Eden 600MHz~2.0GHz CPU.

The VIA CX700 with 32/64/128MB shared main memory supports CRT/Panel displays up to 2048 x 1536. It also supports 24-bit single channel/48-bit dual channel LVDS interface supporting up to 1600 x 1200.

System memory is also sufficient with the one SO-DDRII socket that can support up to 1G.

Additional onboard connectors include an advanced USB2.0 port providing faster data transmission. And two RJ-45 connectors for 10/100 Based Ethernet uses. To ensure the reliability in an unmanned or standalone system, the watchdog timer (WDT) onboard 3308220 is designed with software that does not need the arithmetical functions of a real-time clock chip. If any program causes unexpected halts to the system, the onboard WDT will automatically reset the CPU or generate an interrupt to resolve such condition.

1.1 Major Features



The 3308220 comes with the following features:

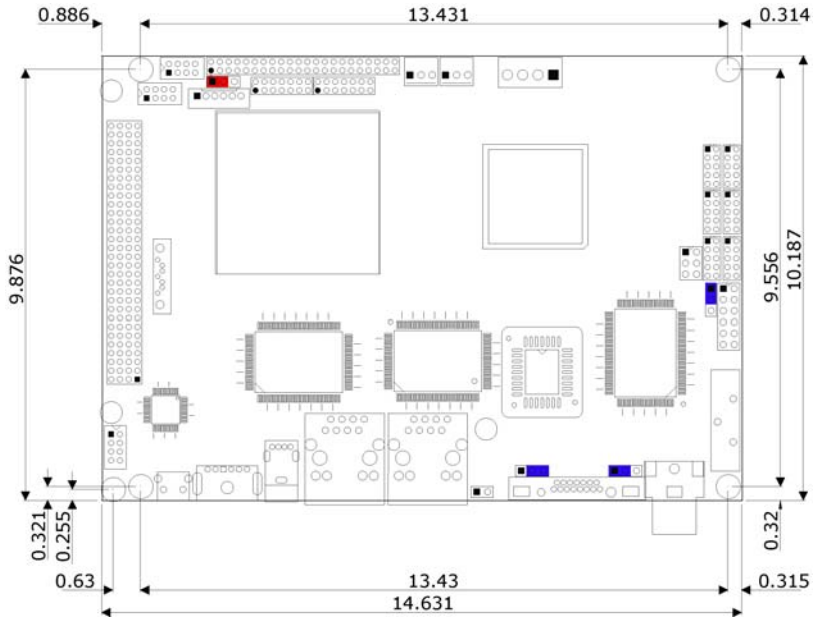
- VIA C7 or ULV VIA V4 Eden processor 600MHz~2.0GHz
- One SO-DDRII socket with a max. capacity of 1GB
- VIA CX700 system chipset
- Winbond W83697UG super I/O chipset
- VIA CX700 graphics controller
- 24-bit/48-bit LVDS Panel display interface
- Dual RealTek RTL8100C Ethernet controller
- VIA VT1708A HD audio controller

- VIA CX700 Serial ATA controller
- Fast PCI ATA/33/66/100 IDE controller
- CF, 8-bit I/O, 4 COM, 5 USB2.0, PC/104 Plus
- +10~+30V wide range single DC power in
- TV-Out, Hardware Monitor function

1.2 Specifications

- **CPU:**
  ULV VIA V4 Eden processor 600MHz/800MHz/1.0GHz
  VIA C7 processor 1.0~2.0GHz
- **Front Side Bus:** Supports 400MHz FSB
- **Memory:** One SO-DDRII socket supports up to 1GB
- **Chipset:** VIA CX700
- **I/O Chipset:** Winbond W83697UG
- **CompactFlash:** One, Type I/II IDE interface adapter
- **8-bit I/O:** 8-bit input/output port (parallel)
- **VGA:** VIA CX700 with 32/64/128MB shared main memory supports CRT display up to 2048 x 1536
- **LVDS Panel:** Supports 24-bit single channel/48-bit dual channel LVDS interface up to 1600 x 1200
- **TV-Out:** Provides PAL or NTSC TV systems
- **Ethernet:** Dual RealTek RTL8100C 10/100 Based LAN
- **Audio:** VIA VT1708A HD audio controller
- **Serial ATA:** VIA CX700 controller with 1 port
- **IDE:** One 2.0-pitch 44-pin IDE connector
- **Serial Port:** 16C550 UART-compatible RS-232/422/485 x 1 and RS-232 x 3 serial ports with 16-byte FIFO
- **PC/104 Plus:** PC/104 Bus connector for PCI Bus
- **USB:** 5 USB2.0 ports, internal x 4 and external x 1
- **Keyboard/Mouse:** PS/2 6-pin Mini DIN
- **BIOS:** AMI PnP Flash BIOS
- **Watchdog Timer:** Software programmable time-out intervals from 1~255 sec.
- **CMOS:** Battery backup
- **Power In:** +10~+30V wide range single DC power in
- **Temperature:** 0~+60°C (operating)
- **Hardware Monitor:** Winbond W83L784R
- **Board Size:** 14.5(L) x 10.2(W) cm

1.3 Board Dimensions



Chapter 2

Unpacking

2.1 Opening the Delivery Package

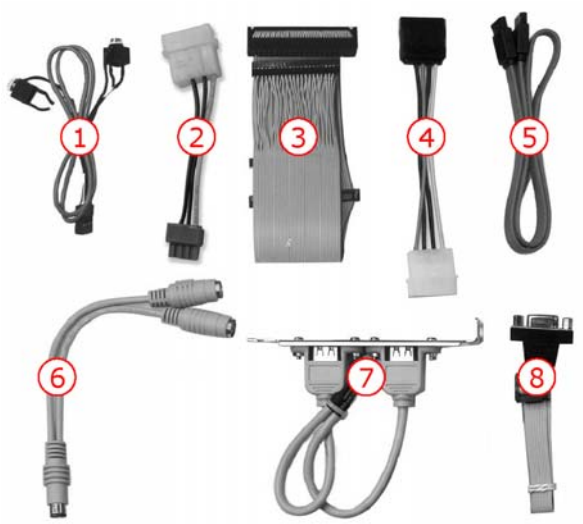
The 3308220 is packed in an anti-static bag. The board has components that are easily damaged by static electricity. Do not remove the anti-static wrapping until proper precautions have been taken. Safety Instructions in front of this manual describe anti-static precautions and procedures.

2.2 Inspection

After unpacking the board, place it on a raised surface and carefully inspect the board for any damage that might have occurred during shipment. Ground the board and exercise extreme care to prevent damage to the board from static electricity.

Integrated circuits will sometimes come out of their sockets during shipment. Examine all integrated circuits, particularly the BIOS, processor, memory modules, ROM-Di sk, and keyboard controller chip to ensure that they are firmly seated. The 3308220 delivery package contains the following items:

- **3308220 Board x 1**
- **Utility CD Disk x 1**
- **Cables Package x 1**
- **Jumper Bag x 1**
- **User's Manual**



Cables Package	
NO.	**Description**
1	Audio cable x 1
2	4-pin power cable x 1
3	IDE flat cable x 1
4	SATA power cable x 1 (optional)
5	SATA cable x 1 (optional)
6	Keyboard/Mouse transfer cable x 1
7	2 USB cable with bracket x 1 (optional)
8	Serial port flat cable x 1

It is recommended that you keep all the parts of the delivery package intact and store them in a safe/dry place for any unforeseen event requiring the return shipment of the product. In case you discover any missing and/or damaged items from the list of items, please contact your dealer immediately.

Chapter 3

Hardware Installation

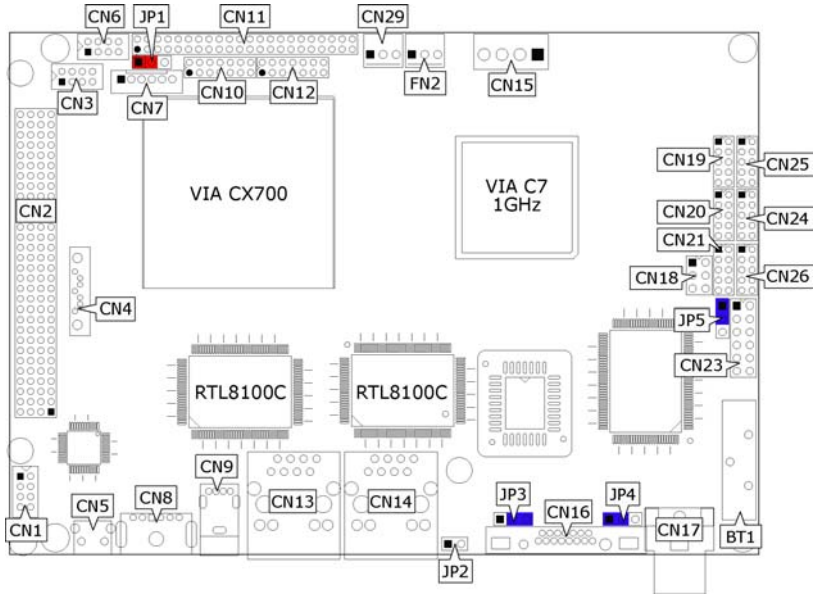
This chapter provides the information on how to install the hardware using the 3308220. This chapter also contains information related to jumper settings of switch, and watchdog timer selection etc.

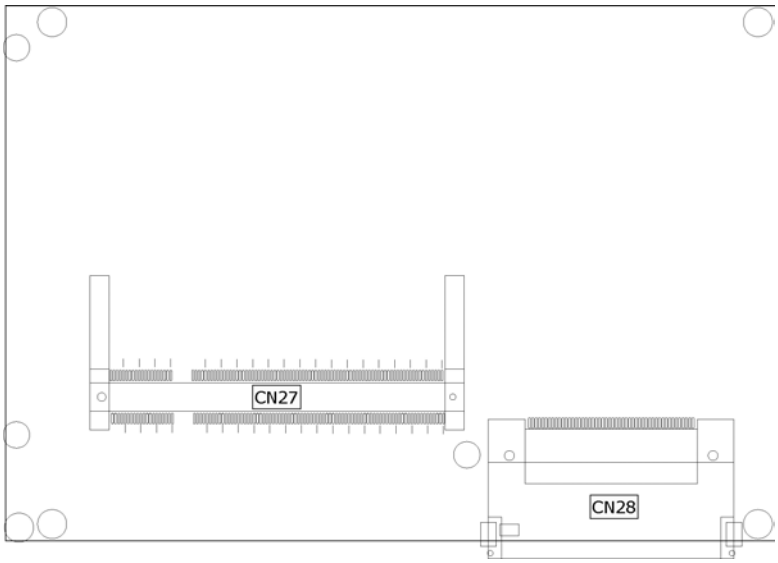
3.1 Before Installation

After confirming your package contents, you are now ready to install your hardware. The following are important reminders and steps to take before you begin with your installation process.

1. Make sure that all jumper settings match their default settings and CMOS setup correctly. Refer to the sections on this chapter for the default settings of each jumper. (JP5 short 1-2)
2. Go through the connections of all external devices and make sure that they are installed properly and configured correctly within the CMOS setup. Refer to the sections on this chapter for the detailed information on the connectors.
3. Keep the manual and diskette in good condition for future reference and use.

3.2 Board Layout





3.3 Jumper List

Jumper	Default Setting	Setting	Page
JP1	Panel Voltage Select: *+3.3V*	Short 1-2	10
JP3	CF Use Master/Slave Select: *Slave*	Short 2-3	22
JP4	Display Out Function Select: *CRT*	Short 1-2	19
JP5	Clear CMOS: *Normal Operation*	Short 1-2	15
CN25	COM2 Use RS-232 or RS-422/485 Select: *RS-232*	Open	13

3.4 Connector List

Connector	Definition	Page
CN1	MIC In/Line Out Connector	21
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CN11	IDE Connector	12
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CN16	15-pin CRT Connector	10
CN17	TV-Out Connector	19
CN18	RS-422/485 Connector	13
CN19	8-bit Input/Output	23
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CN23	System Front Panel Control	16
CN27	SO-DDRII Socket	10
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CN29	External Power In Connector	15
FN2	Fan Power In Connector	15

3.5 Configuring the CPU

The 3308220 embedded with ULV VIA V4 Eden 600MHz/800MHz/ 1GHz or VIA C7 1.0/1.5/2.0GHz CPU. User don't need to adjust the frequently and check speed of CPU.

3.6 System Memory

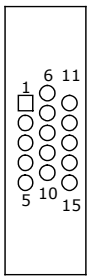
The 3308220 provides one SO-DDRII socket at locations *CN27*. The maximum capacity of the onboard memory is 1GB.

3.7 VGA Controller

The 3308220 provides two connection methods of a VGA device. *CN25* offers an internal 10-pin CRT connector and *CN6/CN9* are the LVDS interface connectors onboard reserved for flat panel installation.

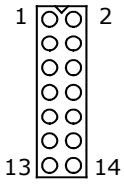
- **CN16: 15-pin CRT Connector**

PIN	Description	PIN	Description
1	Red	2	Green
3	Blue	4	N/C
5	GND	6	GND
7	GND	8	GND
9	N/C	10	GND
11	N/C	12	SDA
13	HSYNC	14	VSYNC
15	SDC		



- **CN10/CN12: LVDS Interface Connector**

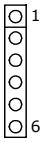
PIN	Description	PIN	Description
1	V_{LCD}	2	V_{LCD}
3	GND	4	GND
5	A0-/B0-	6	A0+/B0+
7	A1-/B1-	8	A1+/B1+
9	A2-/B2-	10	A2+/B2+
11	CLK1-/CLK2-	12	CLK1+/CLK2+
13	A3-/B3-	14	A3+/B3+



NOTE: *LVDS cable should be produced very carefully. A0- & A0+ have to be fabricated in twister pair (A1- & A1+, A2- & A2+ and so on) otherwise the signal won't be stable. Please set the proper voltage of your panel using JP1 before proceeding on installing it.*

- **CN7: Inverter Power In Connector**

PIN	Description
1	+12V
2	+12V
3	VCC
4	BK_EN
5	ENVDD
6	GND



NOTE: *If use CN10 only, it just supports 24-bit single channel LVDS panel; If you want to use 48-bit dual channel LVDS panel, please use CN10 and CN12 combined.*

The 3308220 has an onboard jumper that selects the working voltage of the flat panel connected to the system. Jumper *JP1* offers two voltage settings for the user.

- **JP1: Panel Voltage Select**

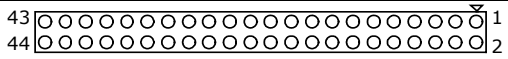
Options	Settings
+3.3V (default)	Short 1-2
+5V	Short 2-3

3.8 IDE Drive Connector

CN11 is a 2.0-pitch 44-pin connector daisy-chain driver connector serves the PCI E-IDE drive provisions onboard the 3308220. A maximum of two ATA/33/66/100 IDE drives can be connected to the 3308220 via *CN11*.

- **CN11: IDE Connector**

PIN	Description	PIN	Description
1	Reset	2	GND
3	PDD7	4	PDD8
5	PDD6	6	PDD9
7	PDD5	8	PDD10
9	PDD4	10	PDD11
11	PDD3	12	PDD12
13	PDD2	14	PDD13
15	PDD1	16	PDD14
17	PDD0	18	PDD15
19	GND	20	N/C
21	PDREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	PIORDY	28	PR1PD1-
29	RPDACK-	30	GND
31	Interrupt	32	N/C
33	RPDA1-	34	PATA66
35	RPDA0-	36	RPDA2-
37	RPCS1-	38	RPCS3-
39	HDD Active	40	GND
41	VCC	42	VCC
43	GND	44	N/C

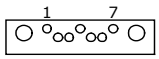


3.9 Serial ATA Connector

You can connect the Serial ATA device that provides you high speeds transfer rates (150MB/sec.). If you wish to use RAID function, please note that these two serial ATA connectors just support RAID0 and only compatible with WIN XP.

- **CN4: Serial ATA Connector**

PIN	Description
1	GND
2	SATATXP
3	SATATXN
4	GND
5	SATARXN
6	SATARXP
7	GND



3.10 Serial Port Connectors

The 3308220 offers NS16C550 compatible UARTs with Read/ Receive 16-byte FIFO serial ports and four internal 10-pin headers and one RS-422/485 connector.

- **CN24/CN20/CN21/CN26: COM 1 ~ COM 4 Connector (5x2 Header)**

PIN	Description	PIN	Description
1	DCD	2	DSR
3	RXD	4	RTS
5	TXD	6	CTS
7	DTR	8	RI
9	GND	10	N/C

- **CN18: RS-422/485 Connector (3x2 Header, COM 2)**

PIN	Description	PIN	Description
1	TX-	2	TX+
3	RX+	4	RX-
5	GND	6	N/C

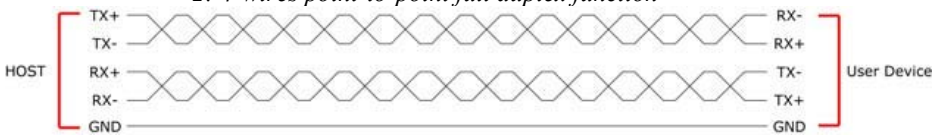
NOTE: *The terminal resistance of RX & TX is set at 180 Ω.*

- **CN25: COM 2 use RS-232 or RS-422/485 Select**

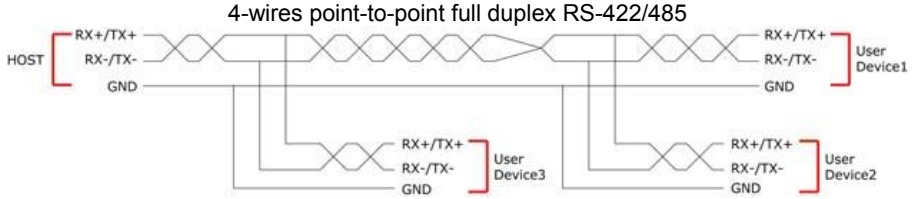
Options	Settings
RS-232 (default)	Open
RS-485 by Auto (*1)	Short 1-2, 3-4, 5-7, 8-10
RS-485 by –RTS (*-1)	Short 1-2, 3-4, 7-9, 8-10
RS-422/485 Full Duplex (*2)	Short 1-2, 3-4, 6-8

NOTE: **1: 2-wires RS-485 function*

**2: 4-wires point-to-point full duplex function*



4-wires point-to-point full duplex RS-422/485



Typical RS-485 2-wires Mutildrop Network

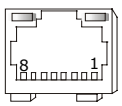
3.11 Ethernet Connector

The 3308220 provides two RJ-45 connectors for 10/100 Based LAN. Please refer to the following for its pin information.

When installs OS, this driver namely can automatically install. User does not need to renewal.

- **CN13/CN14: RJ-45 Connector**

PIN	Description	PIN	Description
1	TCT	10	TX+
2	TX-	11	RX+
3	RX-	12	N/C
4	N/C	13	N/C
5	N/C	14	RCT
6	Link LED	15	330Ω pull VCC3
7	ACT LED	16	330Ω pull VCC3
8	SHIELD	17	SHIELD
9	SHIELD	18	SHIELD



3.12 USB Port

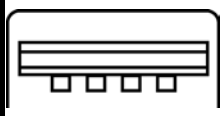
The 3308220 provides three 8-pin connectors, at location *CN21~CN23*, for six USB2.0 ports.

- **CN3/CN6: Internal USB2.0 Connector**

PIN	Description	PIN	Description
1	VCC	2	VCC
3	USBD0- USBD2-	4	USBD1- USBD3-
5	USBD0+ USBD2+	6	USBD1+ USBD3+
7	GND	8	GND

- **CN9: External USB2.0 Port**

PIN	Description
1	VCC
2	BD4-
3	BD4+
4	GND



3.13 CMOS Data Clear

The 3308220 has a Clear CMOS jumper on *JP5.*

- **JP5: Clear CMOS**

Options	Settings
Normal Operation (default)	Short 1-2
Clear CMOS	Short 2-3

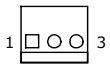
IMPORTANT: *Before you turn on the power of your system, please set JP5 to Short 1-2 for normal operation.*

3.14 Power and Fan Connectors

3308220 provides one 4-pin power in at *CN15*, one 3-pin power in at *CN29*. Connector *FN2* onboard 3308220 is a 3-pin fan power output connector.

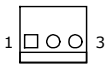
- **CN29: 3-pin Power In Connector**

PIN	Description
1	GND
2	+12V
3	-12V



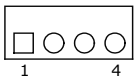
- **FN2: Fan Power In Connector**

PIN	Description
1	GND
2	VCC
3	Fan In



- **CN15: 4pin Power In Connector**

PIN	Description
1	DC In
2	GND
3	GND
4	DC In

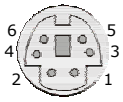


3.15 Keyboard/Mouse Connectors

The *CN8* is a PS/2 6-pin Mini DIN connector for 3308220.

- **CN8: PS/2 6-pin Mini DIN Keyboard/Mouse Connector**

PIN	Description
1	Keyboard Data
2	Mouse Data
3	GND
4	+5V
5	Keyboard Clock
6	Mouse Clock

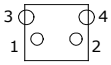


3.16 System Front Panel Control

The 3308220 has front panel control at location *CN23* that indicates the power-on status.

- **CN5: External Reset Button**

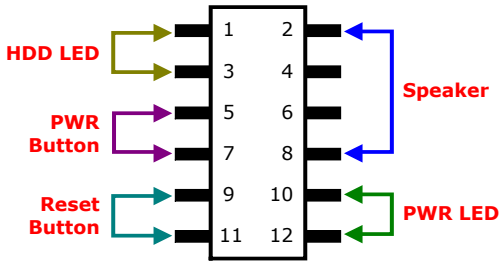
PIN	Description
1	GND
2	Reset Switch
3	GND
4	GND



- **CN23: System Front Panel Control**

PIN	Description	PIN	Description
1	330Ω pull VCC	2	Speaker
3	HDD LED	4	N/C
5	PWR Button	6	GND
7	GND	8	330Ω pull VCC
9	Reset Switch	10	330Ω pull 3.3V
11	GND	12	GND

Connector CN23 Orientation



3.17 Watchdog Timer

Once the Enable cycle is active a Refresh cycle is requested before the time-out period. This restarts counting of the WDT period. When the time counting goes over the period preset of WDT, it will assume that the program operation is abnormal. A reset system signal will restart when such error happens.

The following sample programs show how to enable, disable and refresh the watchdog timer:

```
.286

    .MODEL SMALL
    .DATA                       ;this is data area

x1          db '-----------------------------------------------------',0ah,0dh,'$'
copyright   db '|Copyright by Global American, Inc.              |',0ah,0dh,'$'
x2          db '-----------------------------------------------------',0ah,0dh,'$'
```

```
port    equ     04Eh    ;W83697H Chipset port
datao   equ     04Fh    ;data port

        .CODE

print   macro   buff
        mov     dx,offset buff;
        mov     ah,09h
        int     21h
        endm

begin   proc    near
        mov     ax,@data
        mov     ds,ax
      STI
                ; W83697H
        mov     dx,port     ; Unlock registor
        mov     al,087H     ;
        out     dx,al
        jmp     $+2
        out     dx,al
        mov     dx,port     ;
        mov     al,07H      ;
        out     dx,al
        jmp     $+2
        mov     dx,datao    ; set device 8
        mov     al,08H      ;
        out     dx,al
        jmp     $+2

        mov     dx,port     ; Watchdog IO function
        mov     al,030H     ; registor
        out     dx,al
        jmp     $+2

        mov     dx,datao    ; set 01h toactivate
        mov     al,01H      ;
        out     dx,al
        jmp     $+2

        mov     dx,port     ; set CRF3
        mov     al,0f3H     ;
        out     dx,al
        jmp     $+2

        mov     dx,datao    ; set CRF3 to secend
        mov     al,00H      ;
        out     dx,al
        jmp     $+2

        mov     dx,port     ; set CRF4 time
        mov     al,0f4H     ;
        out     dx,al
        jmp     $+2

        mov     dx,datao    ; set CRF4 time to 5 s'
        mov     al,05H      ;
        out     dx,al

        print   x1
        print   copyright
```

```
        print   x2
        mov     ah,4ch      ;go back to dos
        int     21h
        .stack
begin   endp
        end begin
```

User can also use AL, 00H's defined time for reset purposes, e.g.00H for Disable, 01H = 1sec, 02H=2sec….FFH=255sec.

3.18 TV-Out Function

The 3308220 can support TV-out function whose input could be up to 800 x 600 graphics resolutions. World Wide Video standards are supported including NTSC-M (North America, Taiwan), NTSC-J (Japan), PAL-b, D, G, H, I (Europe, Asia), PAL-M (Brazil), PAL-N (Uruguay, Paraguay) and PAL-NC (Argentina).

- **CN17: TV-Out Connector**

PIN	Description
1	CVBS
2	GND

- **JP4: Display Out Function Select**

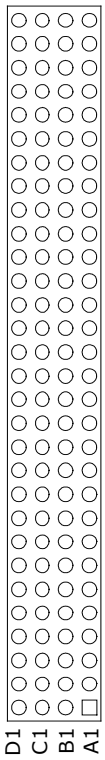
Options	Settings
TV-Out	Short 2-3
CRT (default)	Short 1-2

3.19 PC/104 Plus Connector

The 3308220 provides one PC/104 Plus connector, at location *CN2*.

- **CN2: PC/104 Plus Connector**

PIN	Description	PIN	Description
A1	N/C	B1	N/C
A2	N/C	B2	AD2
A3	AD5	B3	GND
A4	CBE0#	B4	AD7
A5	GND	B5	AD9
A6	AD11	B6	N/C
A7	AD14	B7	AD13
A8	+3.3V	B8	CBE1#
A9	SERR#	B9	GND
A10	GND	B10	PERR#
A11	STOP#	B11	+3.3V
A12	+3.3V	B12	TRDY-
A13	FRAME#	B13	GND
A14	GND	B14	AD16
A15	AD18	B15	+3.3V
A16	AD21	B16	AD20
A17	+3.3V	B17	AD23
A18	IDSEL0	B18	GND
A19	AD24	B19	CBE3#
A20	GND	B20	AD26
A21	AD29	B21	VCC
A22	VCC	B22	AD30
A23	REQ0#	B23	GND
A24	GND	B24	REQB
A25	GNTA	B25	N/C
A26	VCC	B26	PCICLK8
A27	PCICLKB	B27	VCC
A28	GND	B28	INTR_D#
A29	+12V	B29	INTR_A#
A30	-12V	B30	REQC



...MORE ON NEXT PAGE...

PIN	Description	PIN	Description
C1	VCC	D1	AD0
C2	AD1	D2	VCC
C3	AD4	D3	AD3
C4	GND	D4	AD6
C5	AD8	D5	GND
C6	AD10	D6	PULL VCC
C7	GND	D7	AD12
C8	AD15	D8	+3.3V
C9	N/C	D9	PAR
C10	+3.3V	D10	PULL VCC
C11	PULL VCC	D11	GND
C12	GND	D12	DEVSEL#
C13	IRDY#	D13	+3.3V
C14	+3.3V	D14	CBE2#
C15	AD17	D15	GND
C16	GND	D16	AD19
C17	AD22	D17	+3.3V
C18	IDSEL1	D18	IDSEL2
C19	N/C	D19	IDSEL3
C20	AD25	D20	GND
C21	AD28	D21	AD27
C22	GND	D22	AD31
C23	REQA	D23	N/C
C24	VCC	D24	GNT0#
C25	GNTB	D25	GND
C26	GND	D26	PCICLKA
C27	PCICLKC	D27	GND
C28	VCC	D28	PCIRST#
C29	INTR_B#	D29	INTR_C#
C30	INTR_C#	D30	N/C

3.20 Audio Connectors

The 3308220 has an onboard VIA VT1708A High Definition Audio CODEC. The following tables list the pin assignments of the Line In/Audio Out connector.

- 4 stereo DACs support 24-bit, 192KHz samples
- DAC with 100dB S/N Ratio
- 2 stereo ADCs support 24-bit, 192KHz samples

- ADC with 95dB S/N ratio
- 8-channels of DAC support 16/20/24-bit PCM format for 7.1 audio solution

- **CN1: MIC In/Line Out Connector**

PIN	Description	PIN	Description
1	AOUTL	2	AOUTR
3	GND	4	GND
5	MIC IN L	6	MIC IN R
7	GND	8	GND

3.21 CompactFlash™ Connector

The 3308220 also offers a Type I/II CompactFlash™ connector is IDE interface located at the solder side of the board. The designated *CN28* connector, once soldered with an adapter, can hold CompactFlash™ cards of various sizes. Please turn off the power before inserting the CF card.

Inserting a CompactFlash™ card into the adapter is not a difficult task. The socket and card are both keyed and there is only one direction for the card to be completely inserted. Refer to the diagram on the following page for the traditional way of inserting the card.

- **JP3: CF Use Master/Slave Select**

Options	Setting
Master	Short 1-2
Slave (default)	Short 2-3

- **CN28: CompactFlash™ Connector**

PIN	Description	PIN	Description
1	GND	2	DATA3
3	DATA4	4	DATA5
5	DATA6	6	DATA7
7	SDCS1#	8	GND
9	GND	10	GND
11	GND	12	GND
13	VCC	14	GND
15	GND	16	GND
17	GND	18	SDA2
19	SDA1	20	SDA0
21	DATA0	22	DATA1
23	DATA2	24	470Ω pull GND
25	N/C	26	N/C
27	DATA11	28	DATA12
29	DATA13	30	DATA14
31	DATA15	32	SDCS3#
33	N/C	34	UOR
35	IOW	36	EWE0
37	IRQ	38	VCC
39	CS	40	N/C
41	RESET	42	IORDY
43	DACK	44	REQ
45	IDE LED	46	PDIAG
47	DATA8	48	DATA9
49	DATA10	50	GND

NOTE: *When use CF card, IDE device function will be disabled.*

3.22 8-bit I/O Function

The 3308220 offers one 8-bit input/output port by parallel port.

- **CN19: 8-bit Input/Output**

PIN	Description	PIN	Description
1	VCC	2	GND
3	GD0	4	GD4
5	GD1	6	GD5
7	GD2	8	GD6
9	GD3	10	GD7

```
.286

        .MODEL SMALL
        .DATA                           ;this is data area
port    equ     0378h                   ;print port can be change to 278h

        .CODE

print   macro   buff
        mov     dx, offset buff;
        mov     ah,09h
        int     21h
        endm

delay :
        push    cx
        mov     cx,0155h
@@:
        jmp     $+2
        push    cx
        mov     cx,0ffffh

wait1:  loop    wait1
        pop     cx
        loop    @b
        pop     cx
        ret


begin   proc    near
        mov     ax,@data
        mov     ds,ax
        STI

        Mov     dx, port
        Mov     al, 80h                 out     dx, al

;;--------------------
;;ROR
        mov     cx, 08h
@@:
        ror     al, 1
        call    delay
        out     dx, al
        loop    @b
        pop     cx
;;ROL
        push    cx
        mov     cx, 08h
@@:
        rol     al, 1
        out     dx, al
        call delay
        loop    @b
        pop     cx
;;--------------------
;;--------------------
;;ROR
```

```
        mov     cx, 08h
@@:
        ror     al, 1
        call delay
        out     dx, al
        loop    @b
        pop     cx
;;ROL
        push    cx
        mov     cx, 08h
@@:
        rol     al, 1
        out     dx, al
        call delay
        loop    @b
        pop     cx
;;--------------------
;;--------------------
;;ROR
        mov     cx, 08h
@@:
        ror     al, 1
        call delay
        out     dx, al
        loop    @b
        pop     cx
;;ROL
        push    cx
        mov     cx, 08h
@@:
        rol     al, 1
        out     dx, al
        call delay
        loop    @b
        pop     cx
;;--------------------
;;--------------------
;;ROR
        mov     cx, 08h
@@:
        ror     al, 1
        call delay
        out     dx, al
        loop    @b
        pop     cx
;;ROL
        push    cx
        mov     cx, 08h
@@:
        rol     al, 1
        out     dx, al
        call delay
        loop    @b
        pop     cx
;;--------------------
;;--------------------
;;ROR
        mov     cx, 08h
```

```
@@:
        ror         al, 1
        call delay
        out         dx, al
        loop        @b
        pop         cx
;;ROL
        push        cx
        mov         cx, 08h
@@:
        rol         al, 1
        out         dx, al
        call delay
        loop        @b
        pop         cx
;;--------------------
;;--------------------
;;ROR
        mov         cx, 08h
@@:
        ror         al, 1
        call delay
        out         dx, al
        loop    @b
        pop         cx
;;ROL
        push        cx
        mov         cx, 08h
@@:
        rol         al, 1
        out         dx, al
        call delay
        loop        @b
        pop         cx
;;--------------------
;;--------------------
;;ROR
        mov         cx, 08h
@@:
        ror         al, 1
        call delay
        out         dx, al
        loop        @b
        pop         cx
;;ROL
        push        cx
        mov         cx, 08h
@@:
        rol         al, 1
        out         dx, al
        call delay
        loop        @b
        pop         cx
;;--------------------

;flash LED 3 time
        mov         cx, 01h
@@:
```

```
        mov     al, 0ffh
        out     dx, al
        call delay
        mov     al,0h
        out     dx, al
        call delay
        loop    @b
ee:

        mov     ah, 4ch             ;go back to dos
        int     21h
        .stack
        begin   endp
        end begin
```

Chapter 4

AMI BIOS Setup

The 3308220 uses AMI BIOS for the system configuration. The AMI BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options that could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

4.1 Starting Setup

The AMI BIOS is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

1. By pressing <Del> immediately after switching the system on, or
2. By pressing the <Del> key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP.

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will be asked to...

PRESS F1 TO CONTINUE, DEL TO ENTER SETUP

4.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the <PageUp> and <PageDown> keys to change entries, and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

↑	Move to previous item
↓	Move to next item
←	Move to previous item
→	Move to previous item
Esc key	Main Menu -- Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu
PgUp key	Decrease the numeric value or make changes
PgDn key	Increase the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	Reserved
F2 key	Change color from total 8 colors. F2 to select color forward
F3 key	F2 to select color backward
F4 key	Reserved
F5 key	Reserved
F6 key	Reserved
F7 key	Reserved
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

4.3 Main Menu

Once you enter the AMI BIOS CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to enter the sub-menu.

BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

System Overview

AMI BIOS

Version : 08.00.13
Build Date : 06/13/07
ID : HS261300

Processor

Type : VIA Esther processor 1000MHz
Speed : 1000MHz
Count : 1

System Memory

Size : 504MB

System Time [00:29:32]
System Date [Tue 01/01/2002]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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NOTE: *A brief description of the highlighted choice appears at the bottom of the screen.*

4.4 Advanced Settings

This section allows you to configure your system for the basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.

BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

Advanced Settings

WARNING: Setting wrong values in below sections may cause system to malfunction.

- ▶ CPU Configuration
- ▶ IDE Configuration
- ▶ SuperIO Configuration
- ▶ ACPI Configuration
- ▶ APM Configuration
- ▶ Hardware Health Configuration
- ▶ USB Configuration

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

Configure advanced CPU settings

Module Version –13.00

Manufacturer	:	VIA
Brand String	:	VIA Esther processor 1000MHz
Frequency	:	1.00GHz
FSB Speed	:	400MHz
Cache L1	:	128 KB
Cache L2	:	128 KB
Ratio Status	:	Unlocked (Max:10, Min:08)
Ratio Actual Value	:	10
CMPXCHG8B instruction support		[Enabled]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

IDE Configuration

Parallel ATA IDE device			
► Primary IDE Master	:	[Not Detected]	
► Primary IDE Slave	:	[Not Detected]	
► Secondary IDE Master	:	[Not Detected]	
► Secondary IDE Slave	:	[Not Detected]	
Parallel ATA IDE Controller		[Both]	
Hard Disk Write Protect		[Disabled]	← Select Screen
IDE Detect Time Out (Sec)		[35]	↑↓ Select Item
ATA(PI) 80Pin Cable Detection		[Host]	+ - Change Field
			Tab Select Field
			F1 General Help
			F10 Save and Exit
			ESC Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

Configure WIN697UF Super IO Chipset

Serial Port1 Address	[3F8/IRQ4]	
Serial Port2 Address	[2F8/IRQ3]	
Serial Port3 Address	[3E8]	
Serial Port3 IRQ Select	[IRQ11]	
Serial Port4 Address	[2E8]	
Serial Port4 IRQ Select	[IRQ10]	← Select Screen
Parallel Port Address	[378]	↑↓ Select Item
Parallel Port Mode	[Normal]	+ - Change Field
Parallel Port IRQ	[IRQ7]	Tab Select Field
		F1 General Help
		F10 Save and Exit
		ESC Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

ACPI Settings

ACPI Aware O/S	[No]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

Power Management/APM	[Enabled]		
Power Button Mode	[On/Off]		
Suspend Power Saving Type	[C3]		
Restore on AC/Power Loss	[Power On]		
Manual Throttle Ratio	[50%-56.25%]		
System Thermal	[Disabled]		
Thermal Active Temperature	[65°C/149°F]		
THRM throttle Ratio	[50%-56.25%]		
Standby Time Out	[Disabled]		
Suspend Time Out	[Disabled]		
Hard Disk Time Out (Minute)	[Disabled]		
Green PC Monitor Power State	[Suspend]		
Video Power Down Mode	[Suspend]		
Hard Disk Power Down Mode	[Suspend]		
Advanced Monitor Events Controls			
Display Activity	[Ignore]		
Monitor IRQ3	[Monitor]		
Monitor IRQ4	[Ignore]		
Monitor IRQ5	[Ignore]		
Monitor IRQ7	[Ignore]		
Monitor IRQ9	[Ignore]		
Monitor IRQ10	[Ignore]		
Monitor IRQ11	[Ignore]		
Monitor IRQ13	[Ignore]		
Monitor IRQ14	[Monitor]		
Monitor IRQ15	[Ignore]		
Advanced Resume Events Controls		←	Select Screen
Resume On Ring	[Disabled]	↑ ↓	Select Item
Resume On PME#	[Disabled]	+ -	Change Field
Resume On KBC	[Disabled]	Tab	Select Field
Wake-Up Key	[Any Key]	F1	General Help
Resume On PS/2 Mouse	[Disabled]	F10	Save and Exit
Resume On RTC Alarm	[Disabled]	ESC	Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

USB Configuration

Module Version – 2.24.0-11.4

USB Devices Enabled:
None

USB 1.1 Ports Configuration	[USB 6 Ports]		
USB 2.0 Ports Enable	[Enabled]		
Legacy USB Support	[Enabled]	←	Select Screen
USB 2.0 Controller Mode	[FullSpeed]	↑↓	Select Item
		+ -	Change Field
		Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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BIOS SETUP UTILITY

Main	**Advanced**	PCIPnP	Boot	Security	Chipset	Exit

H/W Health Function	[Enabled]		
CPU Temperature	:		
System Temperature	:		
Fan 1 Reading	:		
	:		
Vcore(VIN1)	:		
+3.3V(VIN2)	:	←	Select Screen
VBAT(VIN3)	:	↑↓	Select Item
VCC	:	+ -	Change Field
		Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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4.5 Advanced PCI/PnP Settings

This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system that allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Advanced PCI/PnP Settings

WARNING: Setting wrong values in below sections may cause system to malfunction.

Clean NVRAM	[No]		
Plug & Play O/S	[No]		
PCI Latency Timer	[64]		
Allocate IRQ to PCI VGA	[Yes]		
Palette Snooping	[Disabled]		
PCI IDE BusMaster	[Disabled]		
Offboard PCI/ISA IDE Card	[Auto]		
IRQ3	[Available]		
IRQ4	[Available]		
IRQ5	[Available]		
IRQ7	[Available]		
IRQ9	[Available]		
IRQ10	[Available]		
IRQ11	[Available]		
IRQ14	[Available]		
IRQ15	[Available]		
DMA Channel 0	[Available]		
DMA Channel 1	[Available]	←	Select Screen
DMA Channel 3	[Available]	↑ ↓	Select Item
DMA Channel 5	[Available]	+ -	Change Field
DMA Channel 6	[Available]	Tab	Select Field
DMA Channel 7	[Available]	F1	General Help
		F10	Save and Exit
Reserved Memory Size	[Disabled]	ESC	Exit

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4.6 Boot Settings

BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Boot Settings

► Boot Settings Configuration

► Boot Device Priority
► Removable Drives

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Boot Settings Configuration

Quick Boot	[Enabled]
Quiet Boot	[Disabled]
AddOn ROM Display Mode	[Force BIOS]
Bootup Nom-Lock	[On]
PS/2 Mouse Support	[Auto]
Wait For 'F1' If Error	[Enabled]
Hit 'DEL' Message Display	[Enabled]
Interrupt 19 Capture	[Disabled]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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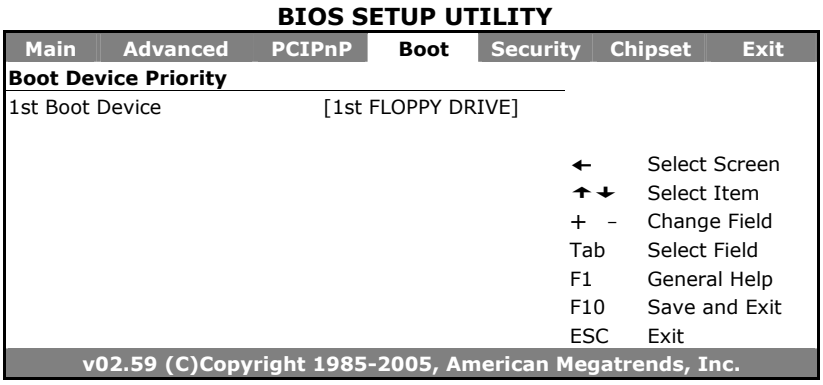
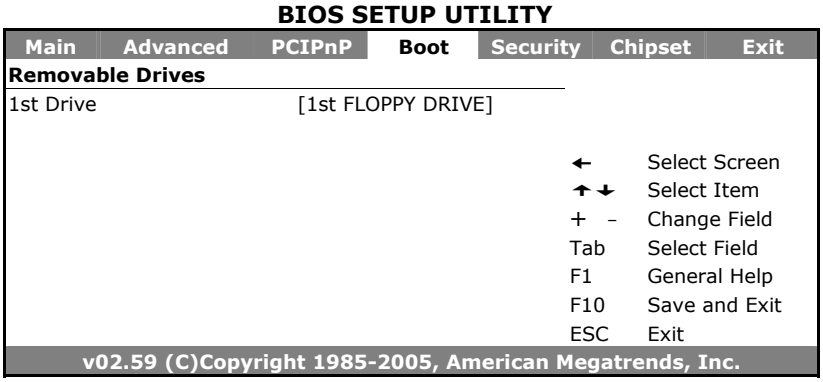
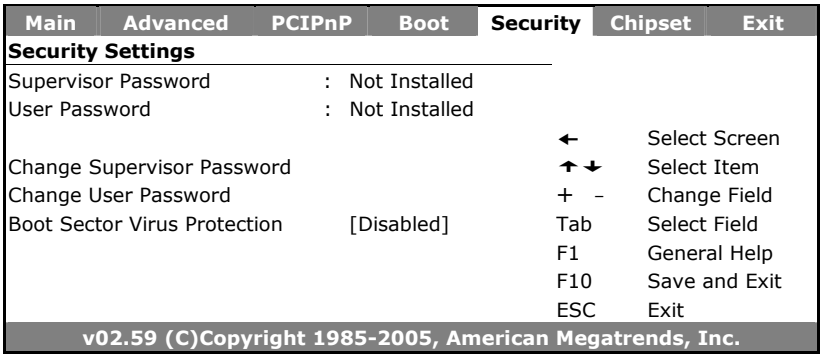




4.7 Security Settings



4.8 Advanced Chipset Settings

BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

Advanced Chipset Settings

WARNING: Setting wrong values in below sections may cause system to malfunction.

► NorthBridge VIA CX700 Configuration
► SouthBridge VIA CX700 Configuration

←	Select Screen
↑↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

NorthBridge VIA CX700 Configuration

► DRAM Clock/Timing Configuration
► AGP & P2P Bridge Configuration
► V-Link & PCI Bus Configuration

Top Performance	[Disabled]		
Software Reset E2 issue	[Escape Patch]	←	Select Screen
Change DCLK using RDCKM	[Program]	↑↓	Select Item
► OnChip VGA Configuration		+ -	Change Field
		Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

DRAM Frequency/Timing Configuration

DRAM Frequency	[Auto]
DRAM Timing	[Auto]
DRAM Command Rate	[2T Command]
RDSAIT/RDSBIT mode	[Auto]
Memory Chip Driving	[Normal]
DDR2 Memory Chip ODT	[Auto]
DDR DQSBAR	[Disabled]
BA0 SEL	[A13]
BA1 SEL	[A14]
BA2 SEL	[A15]
BA Scramble	[Disabled]
DQSO scanning mode	[Disabled]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

AGP & P2P Bridge Configuration

Primary Graphics Adapter	[PCI]
AGP Aperture Size	[128MB]
AGP 3.0 Mode	[8X]
AGP Driving Control	[Auto]
AGP Fast Write	[Enabled]
AGP Master 1 WS Read	[Disabled]
AGP Master 1 WS Write	[Disabled]
AGP 3.0 Calibration cycle	[Disabled]

←	Select Screen
↑ ↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
ESC	Exit

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BIOS SETUP UTILITY

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

V-Link & PCI Bus Configuration

PCI Master 0 WS Write	[Enabled]		
V-Link mode selection	[Auto]		
V-Link 8X Supported	[Enabled]		
V-Link Data 2X Support	[Disabled]		
DRDY Timing	[Default]		
RCONV	[Enabled]	←	Select Screen
Dynamic CKE select	[Auto]	↑↓	Select Item
Dynamic Clock Stop Control	[00]	+ -	Change Field
PCI Read Caching Select	[EE]	Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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OnChip VGA Configuration

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

VGA Frame Buffer Size	[64MB]		
CPU Direct Access Frame Buffer	[Enabled]		
Select Display Device	[CRT]		
Panel Type	[01:800X600]	←	Select Screen
TV H/W Layout	[Default]	↑↓	Select Item
TV Type	[NTSC]	+ -	Change Field
TV Output Connector	[CVBS (Composite)]	Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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SouthBridge VIA CX700 Configuration

Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit

* High Definition Audio	[Auto]		
PCI Delay Transaction	[Disabled]	←	Select Screen
		↑↓	Select Item
		+ -	Change Field
		Tab	Select Field
		F1	General Help
		F10	Save and Exit
		ESC	Exit

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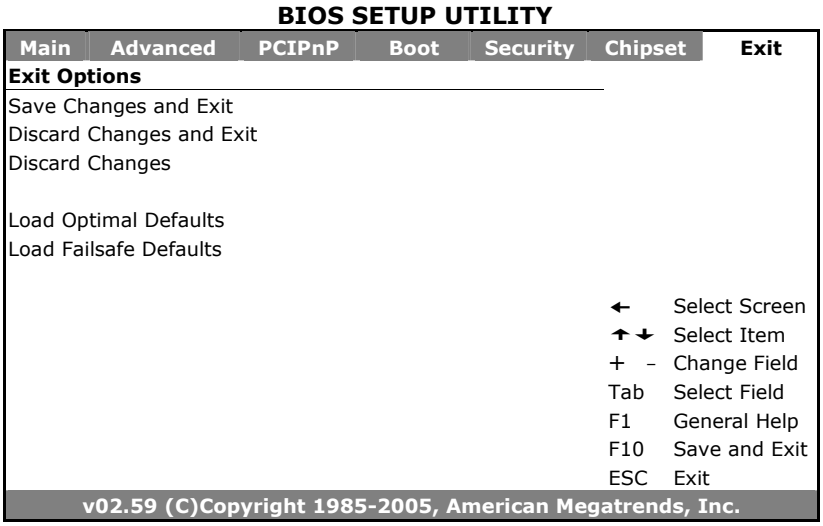
4.9 Exit Options



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