3308560

Wide Range Temperature
Half Size ATOM™ N270 ISA SBC

User's Manual

Version 1.0

2009.12

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Table of Contents

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Chapter 1

Introduction

1.1 Copyright Notice

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.
Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

1.2 About this User's Manual

This User's Manual is intended for experienced users and integrators with hardware knowledge of personal computers. If you are not sure about any description in this User's Manual, please consult your vendor before further handling.

1.3 Warning

Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system

1.4 Replacing the lithium battery

Incorrect replacement of the lithium battery may lead to a risk of explosion. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.
Do not throw lithium batteries into the trashcan. It must be disposed of in accordance with local regulations concerning special waste.

1.5 Technical Support

If you have any technical difficulties, please do not hesitate to call or e-mail our customer service.

1.6 Warranty

This product is warranted to be in good working order for a period of two years from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

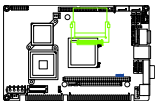
Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Vendors disclaim all other warranties, either expressed or implied, including but not limited to implied warranties of merchantibility and fitness for a particular purpose, with respect to the hardware, the accompanying product's manual(s) and written materials, and any accompanying hardware. This limited warranty gives you specific legal rights.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

1.7 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

	1 x 3308560 half-size ISA Single Board Computer with heatsink
	1 x Driver CD 1 x Quick Installation Guide
Cable Kit	2 x USB Cables 2 x SATA Cables 1 x LPT Cable 1 x KB/MS Y-Cable 1 x IDE Cable 2 x COM Cables

If any of the above items is damaged or missing, contact your vendor immediately.

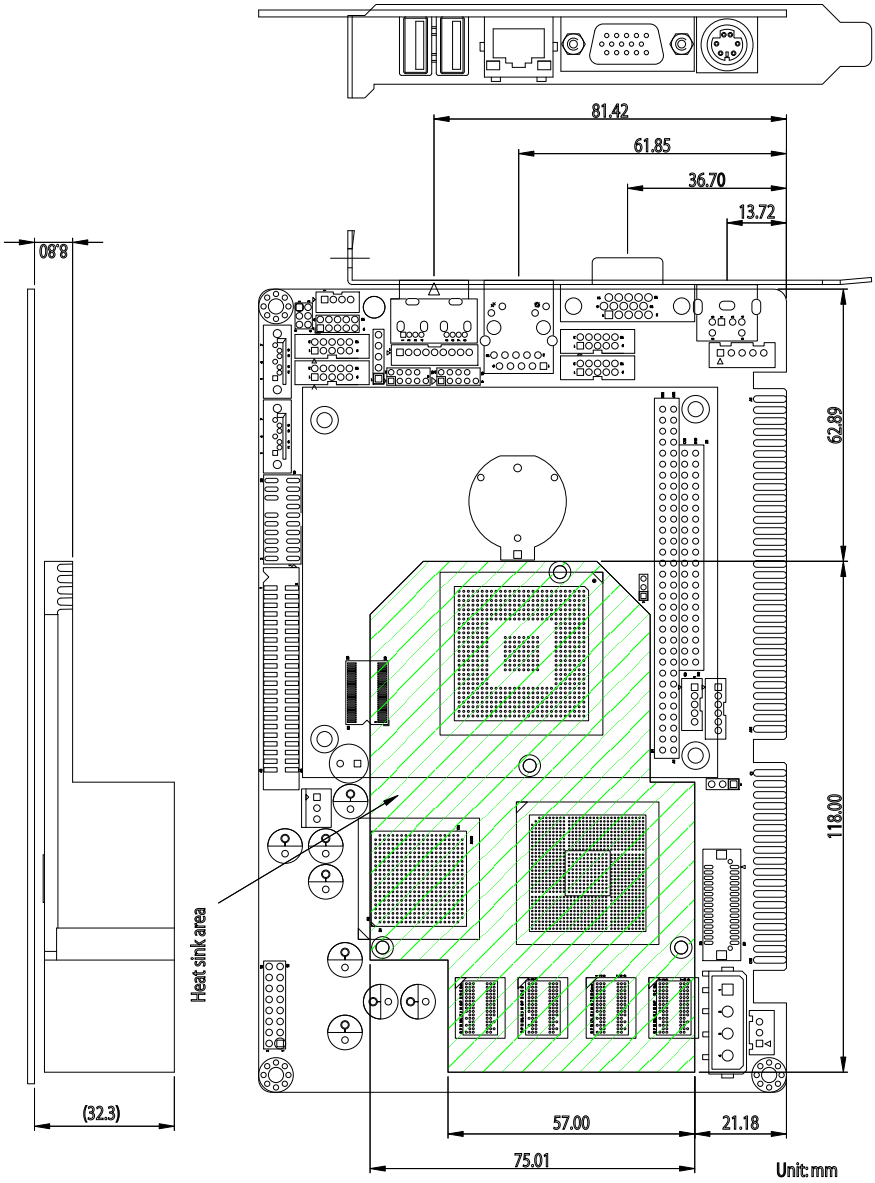
1.8 Ordering Information

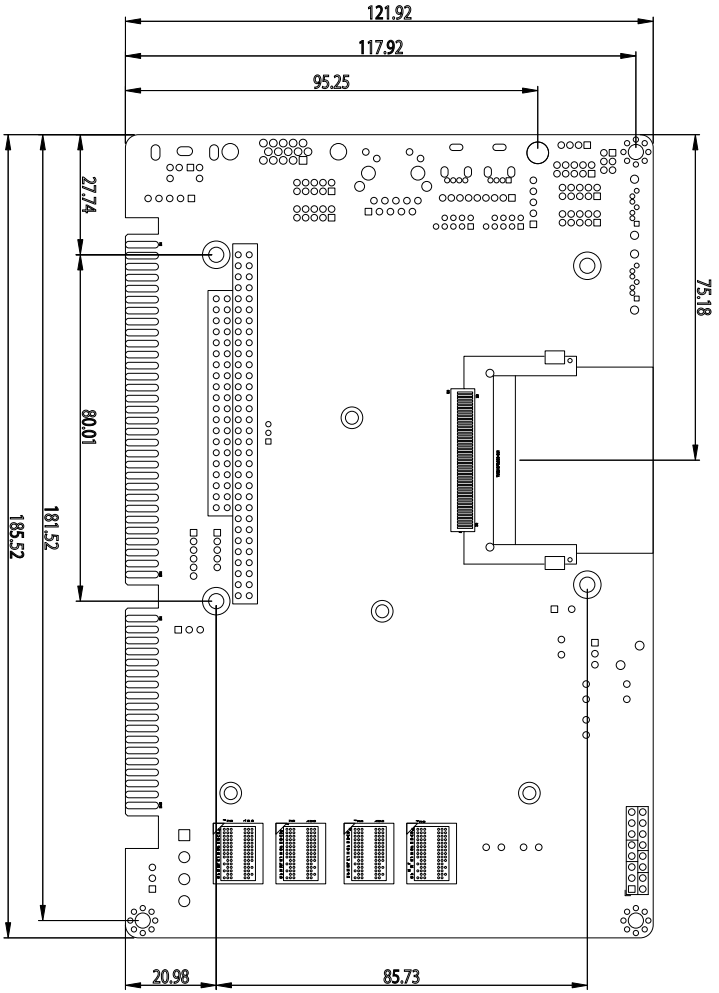
3308560	Intel® Atom™ N270 1.6GHz ISA SBC with 512MB
	Realtek ALC655 AC97 Audio daughter board
	Realtek ALC888 HD Audio daughter board

1.9 Specifications

Form Factor	Half-size ISA Single Board Computer
CPU	Soldered onboard Intel® Atom™ N270 1.6GHz processor
Chipset	Intel® 945GSE + Intel® ICH7M
System Memory	Soldered onboard 512MB DDRII SDRAM with 533MHz, memory capacity up to 1GB
VGA/ LCD Controller	Mobile Intel® Graphics Media Accelerator GMA950 graphics core with Analog RGB/ Dual Channels LVDS
Ethernet	1 x Realtek 8111C PCIe Gigabit Ethernet Controller
I/O Chips	Winbond W83627UHG
BIOS	AMI Flash BIOS
Audio	Supports AC97 or HD Audio via daughter board
Serial ATA	2 x Serial ATA with 150MB/s HDD transfer rate
Serial Port	4 x COM ports (COM1, 3, 4: RS-232, COM2: RS-232/422/485 selectable)
Parallel Port	1 x LPT Port, SPP/EPP/ECP mode selectable
KBMS	Standard PS/2 Keyboard and Mouse via Y-cable
Universal Serial Bus	6 x USB 2.0 ports
Expansion Interface	ISA bus, PC/104 interface
Operation Temp.	-40^{o}C ~ 85^{o}C (-40^{o}F ~ 185^{o}F)
Watchdog Timer	1~255 levels Reset
Dimension (L x W)	185 x 122 mm (7.3” x 4.8”)

1.10 Board Dimensions




121.92
117.92
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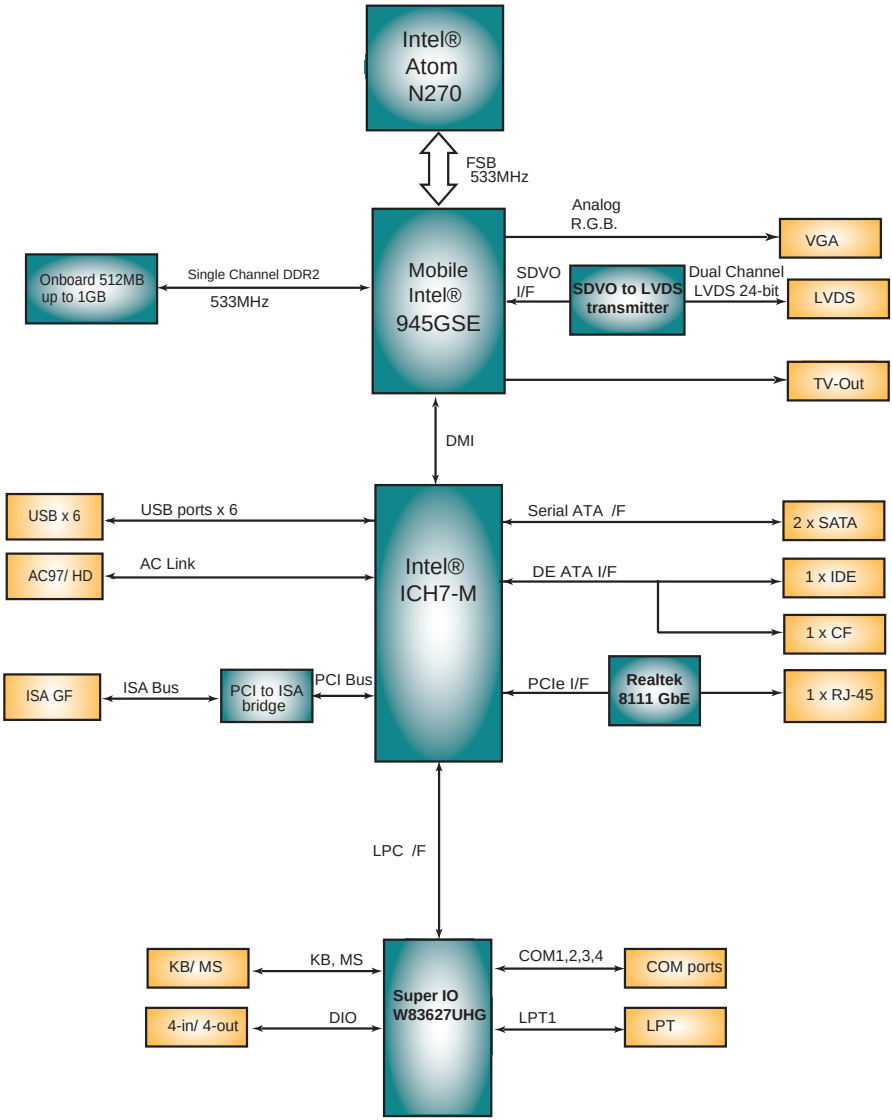
185.52
75.18
20.98
85.73

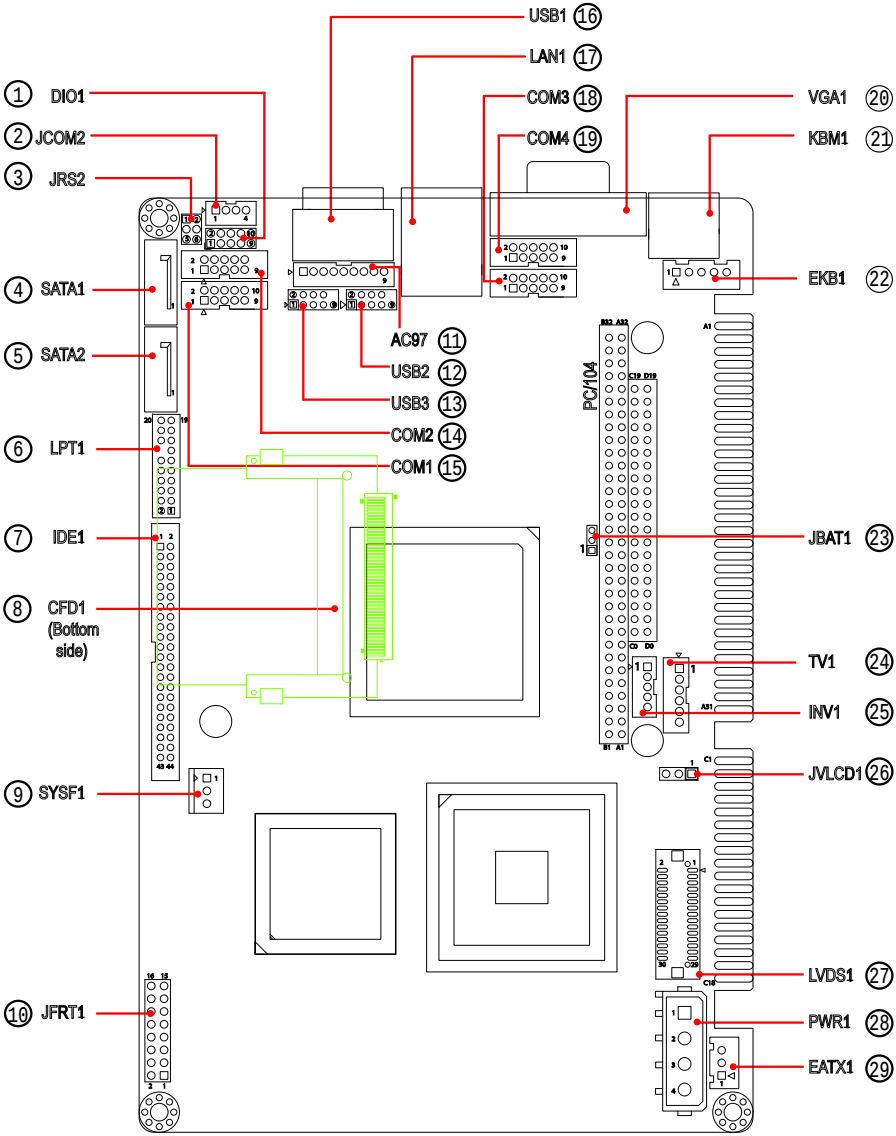
Chapter 2

Installation

2.1 Block Diagram



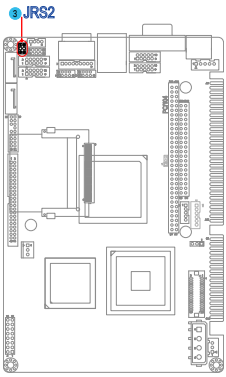
2.2 Jumpers and Connectors



Jumpers

JRS2: COM2 RS-232/422/485 Mode Selection (3)

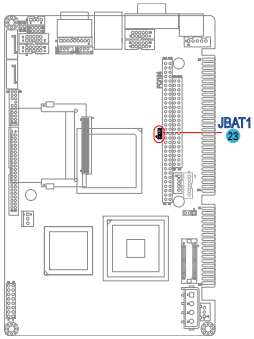
The onboard COM2 port can be configured to operate in RS-422 or RS-485 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper JRS2 switches between RS-232 or RS-422/485 mode. When JRS2 is set to RS-422 or RS-485 mode, there will be only +12V output let while JRS1 is set. All RS-232/422/482 modes are available on COM2.
It can be configured COM2 to operate in RS-232, RS-422 or RS-485 mode
Connector type: 2.00mm pitch 2x3-pin headers.



Mode	RS-232 (Default)	RS-422	RS-485
1-2	ON	OFF	OFF
3-4	OFF	ON	OFF
5-6	OFF	OFF	ON
			

JBAT1: Clear CMOS Setting (23)

If the board refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values.
Connector type: 2.00 mm pitch 1x3 pin-header



Pin	Mode	
1-2	Keep CMOS (Default)	
2-3	Clear CMOS	

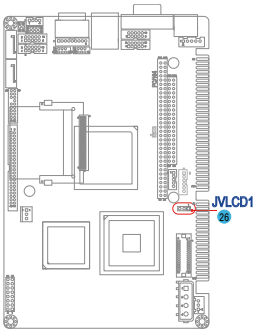
You may need to clear the CMOS if your system cannot boot up because you forgot your password, the CPU clock setup is incorrect, or the CMOS settings need to be reset to default values after the system BIOS has been updated. Refer to the following solutions to reset your CMOS setting:

Solution A:
1. Power off the system and disconnect the power cable.
2. Place a shunt to short pin 1 and pin 2 of JBAT1 for five seconds.
3. Place the shunt back to pin 2 and pin 3 of JBAT1.
4. Power on the system.

Solution B:
If the CPU Clock setup is incorrect, you may not be able to boot up. In this case, follow these instructions:
1. Turn the system off, then on again. The CPU will automatically boot up using standard parameters.
2. As the system boots, enter BIOS and set up the CPU clock.

Note:
If you are unable to enter BIOS setup, turn the system on and off a few times.

JVLCD1: LCD Panel Voltage Selection (26)



The voltage of LCD panel could be selected by JVLCD1 in +5V or +3.3V.

Connector type: 2.54 mm pitch 1x3-pin headers

Pin	Voltage	
1-2	+5V	
2-3	+3.3V (Default)	

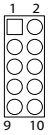
Connectors

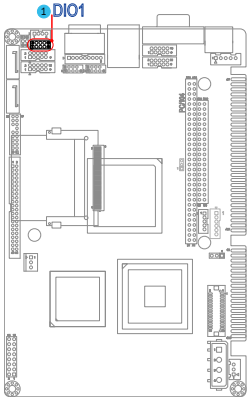
DIO1: Digital I/O Connector (1)

DIO1 is a 8-bit DIO connector that supports 8-bit programmable Input/ Output.

Connector type: 2.00 mm pitch 2x5 pin-header

Pin	Desc.	Pin	Desc.
1	DO0	2	DI0
3	DO1	4	DI1
5	DO2	6	DI2
7	DO3	8	DI3
9	+5V	10	GND

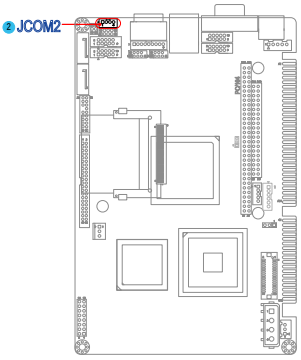




JCOM2: RS-422/ 485 Connector (2)

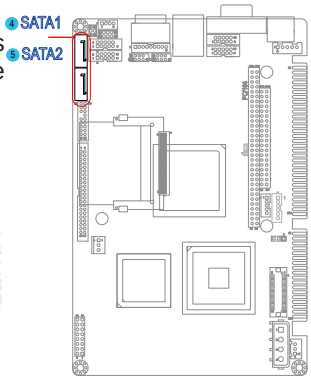
Connector type: 2.00mm pitch
1x4 box wafer connector

Pin	RS-422	RS-485
1	TX+	Data+
2	TX-	Data-
3	RX+	N/C
4	RX-	N/C



SATA1~2: Serial ATA Connectors (4, 5)

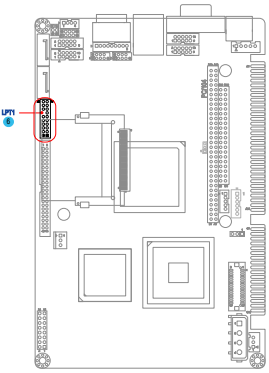
The 3308560 CPU board on board supports two SATA connectors, second generation SATA drives transfer data at speeds as high as 150MB/s, twice the transfer speed of first generation SATA drives.

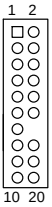


Pin	Description
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

LPT1: Parallel Port Connector (6)

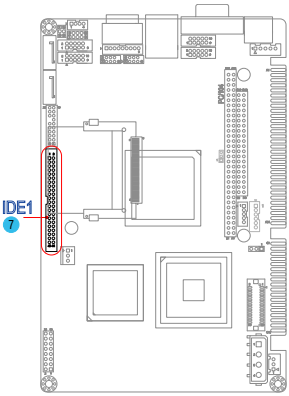
Connector type: 2.00mm pitch 2x10-pin headers.





Pin	Description	Pin	Description
1	STB#	2	AFD#
3	PTD0	4	ERROR#
5	PTD1	6	INIT#
7	PTD2	8	SLIN#
9	PTD3	10	GND
11	PTD4	12	GND
13	PTD5	14	N/C (Key)
15	PTD6	16	Busy
17	PTD7	18	PE
19	ACK#	20	Select

IDE1: Primary IDE Connector (7)

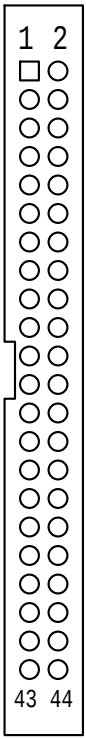


An IDE drive ribbon cable has two connectors to support two IDE devices. If a ribbon cable connects to two IDE drives at the same time, one of them has to be configured as Master and the other has to be configured as Slave by setting the drive select jumpers on the drive.

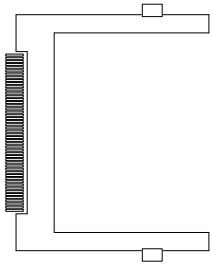
Consult the documentation that came with your IDE drive for details on jumper locations and settings. You must orient the cable connector so that the pin 1 (color) edge of the cable corresponds to pin 1 of the IDE connector.

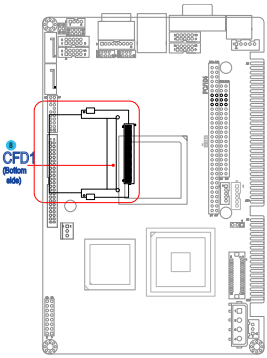
Connector type: 2.00mm pitch 2x22 box headers

Pin	Description	Pin	Description
1	RESET#	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	N/C
21	DREQ	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	IRDY	28	IDSEL
29	ACK#	30	GND
31	IRQ	32	N/C
33	AD1	34	ATA66 DETECT
35	AD0	36	AD2
37	CS#0	38	CS#1
39	ACT#	40	GND
41	+5V	42	+5V
43	GND	44	N/C



CFD1: Compact Flash Type II Socket (8)





Pin	Description	Pin	Description
1	GND	26	GND
2	DATA3	27	DATA11
3	DATA4	28	DATA12
4	DATA5	29	DATA13
5	DATA6	30	DATA14
6	DATA7	31	DATA15
7	CS#1	32	CS#3
8	GND	33	N/C
9	GND	34	IOR#
10	GND	35	IOW#
11	GND	36	+5V
12	GND	37	IRQ14
13	+5V	38	+5V
14	GND	39	CSEL#
15	GND	40	N/C
16	GND	41	IDERST#
17	GND	42	IORDY
18	DA2	43	REQ
19	DA1	44	DACK#
20	DA0	45	DASP
21	DATA0	46	DIAG#
22	DATA1	47	DATA8
23	DATA2	48	DATA9
24	N/C	49	DATA10
25	N/C	50	GND

The interface of Compact Flash socket is designated to use IDE1. The default is setting to IDE Master and Slave with IDE1.

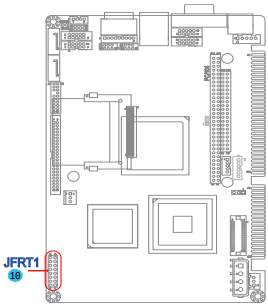
Installation instructions

Compact Flash (CF) card is “not hot-swappable”. If the CF card is swapped in the condition of system power-on, it will damage the CF card.

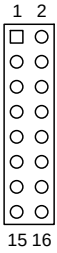
1. Make sure the Single Board Computer is powered OFF.
2. Plug the Compact Flash Type II device into its socket. Verify the direction is correct.
3. Power up the system.

JFRT1: Switches and Indicators (10)

It provides connectors for system indicators that provides light indication of the computer activities and switches to change the computer status.
Connector type: 2.54 mm pitch 2x8 pin header



Pin	Description	Pin	Description
1	Power LED+	2	PWRBTN+
3	GND	4	PWRBTN-
5	GND	6	RESET+
7	HDD LED+	8	RESET-
9	HDD LED-	10	SPEAKER+
11	SMB_CLK	12	SPEAKER+
13	SMB_DATA	14	GND
15	GND	16	+5V



PLED: Power LED Connector, pin 1, 3.

This 2-pin connector connects to the case-mounted power LED. Power LED can be indicated when the CPU card is on or off. And keyboard lock can be used to disable the keyboard function so the PC will not respond by any input.

HLED: HDD LED Connector, pin 7, 9.

This 2-pin connector connects to the case-mounted HDD LED to indicate hard disk activity.

SM Bus: SM Bus connector, pin 11, 13, 15.

PWRBTN: ATX soft power switch, pin 2, 4.

This 2-pin connector connects to the case-mounted Power button.

RES: Reset Button, pin 6, 8.

This 2-pin connector connects to the case-mounted reset switch and is used to reboot the system.

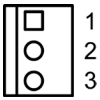
SPK: External Speaker, pin 10, 12, 14, 16.

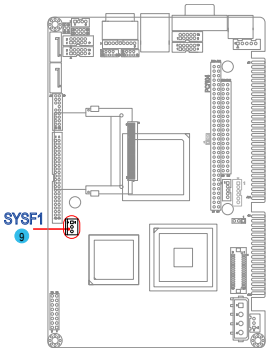
This 4-pin connector connects to the case-mounted speaker.

SYSF1: System Fan Connectors (9)

SYSF1 is a 3-pin header for the system fan. The fan must be a +12V fan.

Pin	Description
1	GND
2	+12V
3	FAN_Speed_Detection



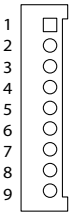


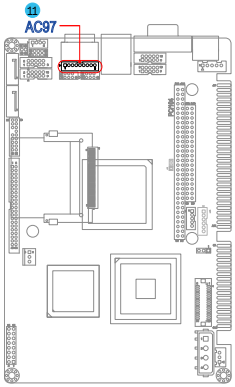
AC97: AUDIO Daughter Board connector (11)

The 3307560 onboard audio connector can connect to an optional audio kit through an onboard audio connector. The CODEC on the optional audio kit is connected to the ICH7M south brigde audio controller through the AC97 or High Definition audio interface.

Connector type: 2.00mm pitch 1x9 box wafer connector.

Pin	Desc.
1	+12V
2	+3.3V
3	AC_SYNC
4	AC_SDOUT
5	GND
6	AC-BCLK
7	GND
8	AC_RST#
9	AC_SDIN0



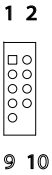


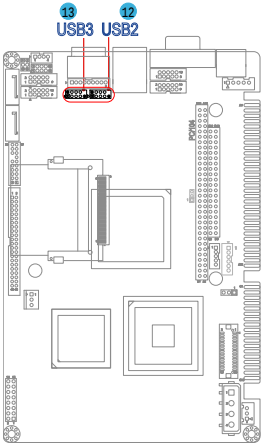
USB2~3: USB Connectors (12, 13)

The 3308560 CPU board on board supports two headers USB2, USB3 that can connect up to 4 high-speed (Data transfers at 480Mb/s), full-speed (Data transfers at 12Mb/s) or low-speed (Data transfers at 1.5Mb/s) USB devices.

Connector type: 2.00mm 2x5-pin headers

Pin	Desc.	Pin	Desc.
1	+5V	2	+5V
3	USBD-	4	USBD-
5	USBD+	6	USBD+
7	GND	8	GND
9	N/C	10	N/C (Key)

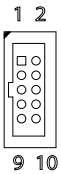


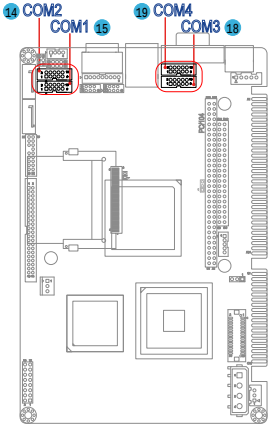


COM1~4: RS-232 Serial Port Connectors (14,15,18,19)

Connector type: 2.00mm pitch 2x5 box-pin headers.

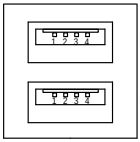
Pin	Desc.	Pin	Desc.
1	DCD#	2	RXD
3	TXD	4	DTR#
5	GND	6	DSR#
7	RTS#	8	CTS#
9	RI#	10	N/C





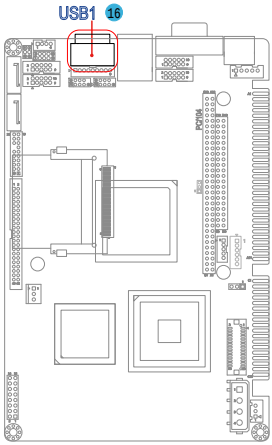
USB1: Double Stacks USB type A connector (16)

The 3308560 CPU board on bracket supports two type A USB connectors that can connect up to two high-speed (Data transfers at 480Mb/s), full-speed (Data transfers at 12Mb/s) or low-speed (Data transfers at 1.5Mb/s) USB devices.
Connector type: double stack USB type A.



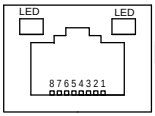
USB

USB

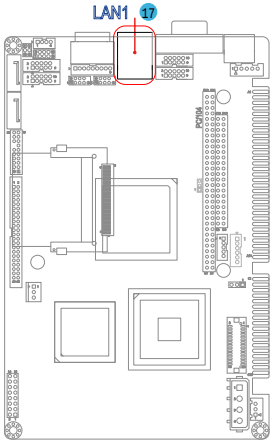


LAN1: Ethernet RJ-45 connector (17)

LAN1 supports one 10/100/1000Mbps Ethernet connector on bracket.
Connector type: RJ-45.



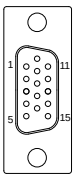
LAN

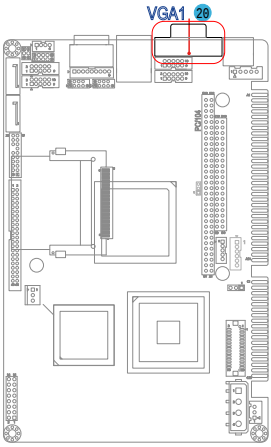


VGA1: Analog RGB Connector (20)

Connector type: D-Sub 15-pin female.

Pin	Description	Pin	Description
1	RED	9	+5V
2	GREEN	10	GND
3	BLUE	11	N/C
4	N/C	12	VDDAT
5	GND	13	HSYNC
6	GND	14	VSYNC
7	GND	15	VDCLK
8	GND		

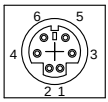




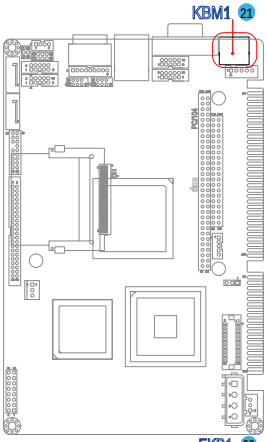
KBM1: Keyboard & Mouse connector (21)

Mini-Din Keyboard & Mouse connector

Pin	Description
1	KB Data
2	MS Data
3	GND
4	+5V
5	KB Clock
6	MS Clock



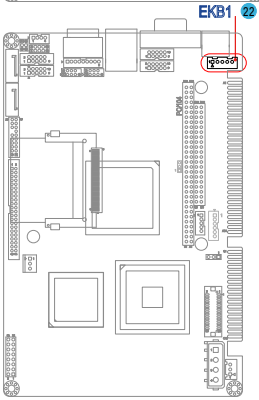
Note: KBM1 supports PS/2 keyboard directly, and PS/2 mouse supported with the additional PS/2 1-to-2 cable in standard packing.



EKB1: External keyboard Connector (22)

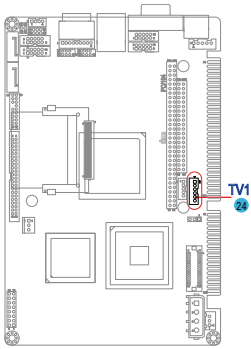
Connector type: 2.54mm pitch 1x5-pin box wafer connector

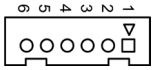
Pin	Description
1	KB_CLK
2	KB_DATA
3	N/C
4	GND
5	+5V



TV1: TV-Out Connector (24)

The TV out connector is for output to a television.
Connector type: 2.00mm pitch 1x6-pin box wafer connector



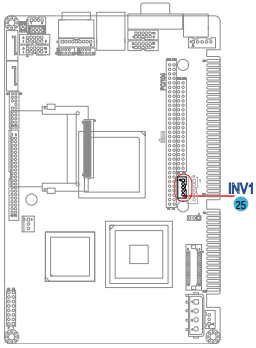


Composite Video			
1	CVBS	2	GND
3	Unused	4	GND
5	Unused	6	GND
S-Video			
1	Unused	2	GND
3	Luminance	4	GND
5	Chrominance	6	GND

INV1: LCD Inverter Connector (25)

Connector type: 2.00mm pitch 1x5-pin box wafer connector.

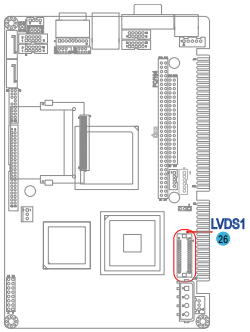
Pin	Description
1	+12V
2	GND
3	Backlight on/off
4	Brightness control
5	GND



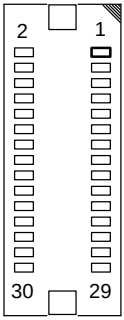
- Backlight signal: The signal sets to high is “On” and low to “Off”. It is used to gate power into the backlight circuitry.
- Brightness control: This signal is used as the PWM Clock input signal.

LVDS1: LVDS Connector (27)

The LVDS connector supports 24-bit LVDS.
VDD could be selected by JVLCD1 in +5V or +3.3V.
Connector type: DF-13-30DP-1.25V



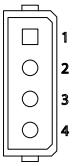
Pin	Description	Pin	Description
2	VDD	1	VDD
4	TX2CLK+	3	TX1CLK+
6	TX2CLK-	5	TX1CLK-
8	GND	7	GND
10	TX2D0+	9	TX1D0+
12	TX2D0-	11	TX1D0-
14	GND	13	GND
16	TX2D1+	15	TX1D1+
18	TX2D1-	17	TX1D1-
20	GND	19	GND
22	TX2D2+	21	TX1D2+
24	TX2D2-	23	TX1D2-
26	GND	25	GND
28	TX2D3+	27	TX1D3+
30	TX2D3-	29	TX1D3-

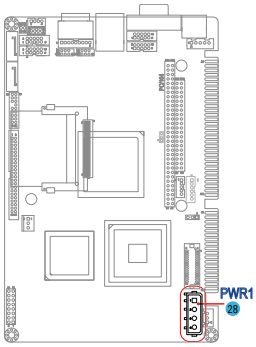


PWR1: Power Supply Connector (28)

Connector type: 5.08mm pitch 1x4-pin connector.

Pin	Description
1	+5V
2	GND
3	GND
4	+12V

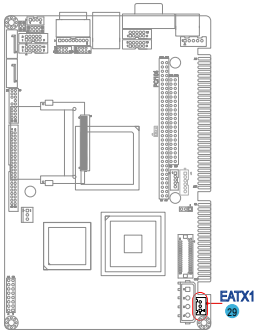




EATX1: ATX Feature Connector (29)

Connector type: 2.54mm pitch 1x3-pin box wafer connector

Pin	Description
1	PS-ON
2	GND
3	5V_SB



2.3 The Installation Paths of CD Driver

Driver	Path
CHIPSET	\CHIPSET\INTEL\INF 9
LAN	\ETHERNET\REALTEK\8111B_WIN5698
VGA	\GRAPHICS\INTEL_2K_XP_32\1432

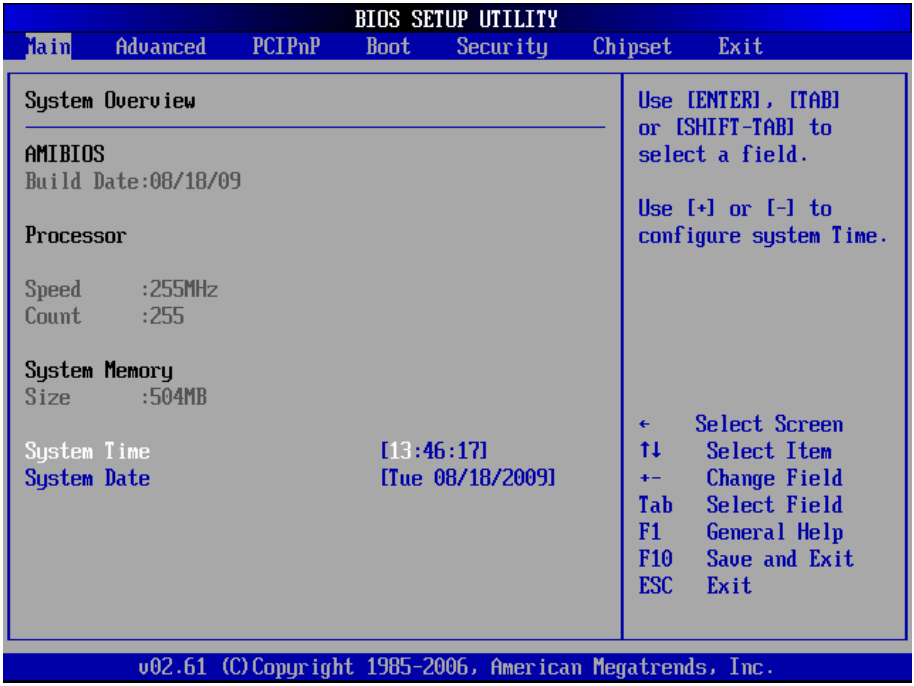
Chapter 3

BIOS

3.1 BIOS Main Setup

The AMI BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility.

When you turn on the computer, the AMI BIOS is immediately activated. The Main allows you to select several configuration options. Use the left/right arrow keys to highlight a particular configuration screen from the top menu bar or use the down arrow key to access and configure the information below.



System Time

Set the system time.

The time format is:

Hour : 00 to 23
Minute : 00 to 59
Second : 00 to 59

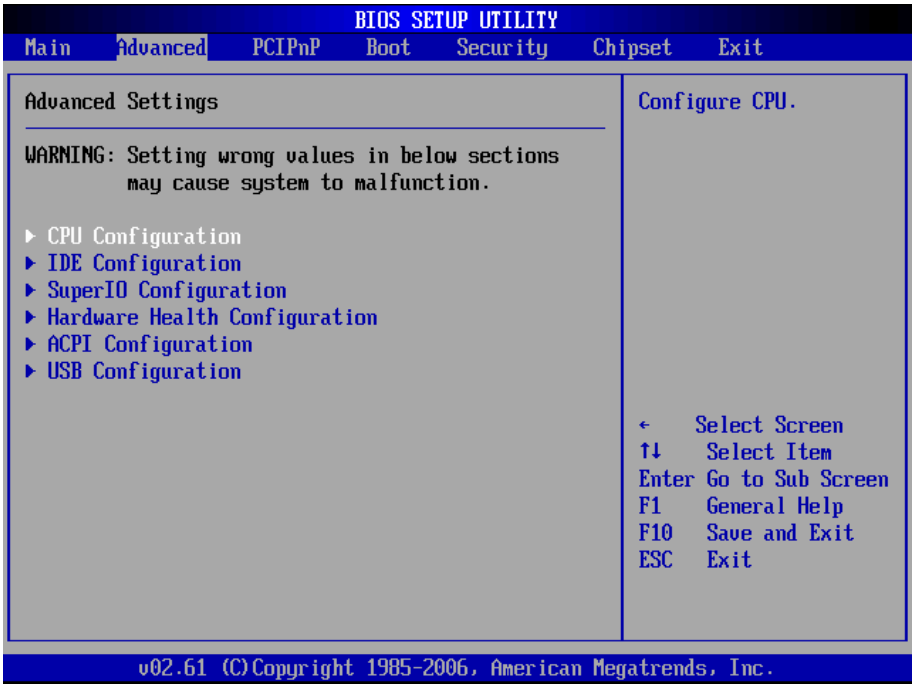
System Date

Set the system date. Note that the 'Day' automatically changes when you set the date.

The date format is:

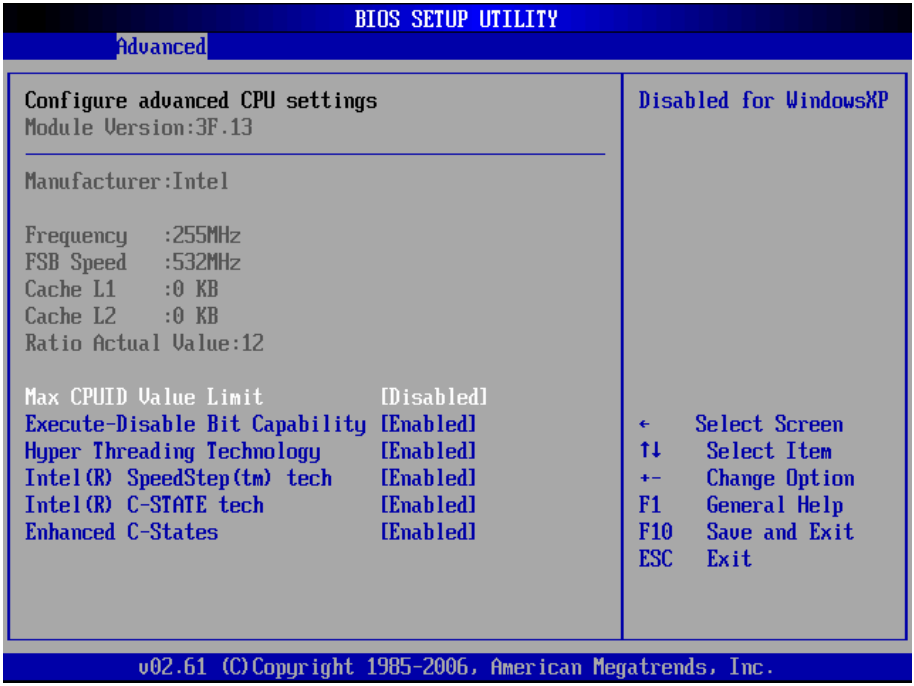
Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

3.2 Advanced Settings

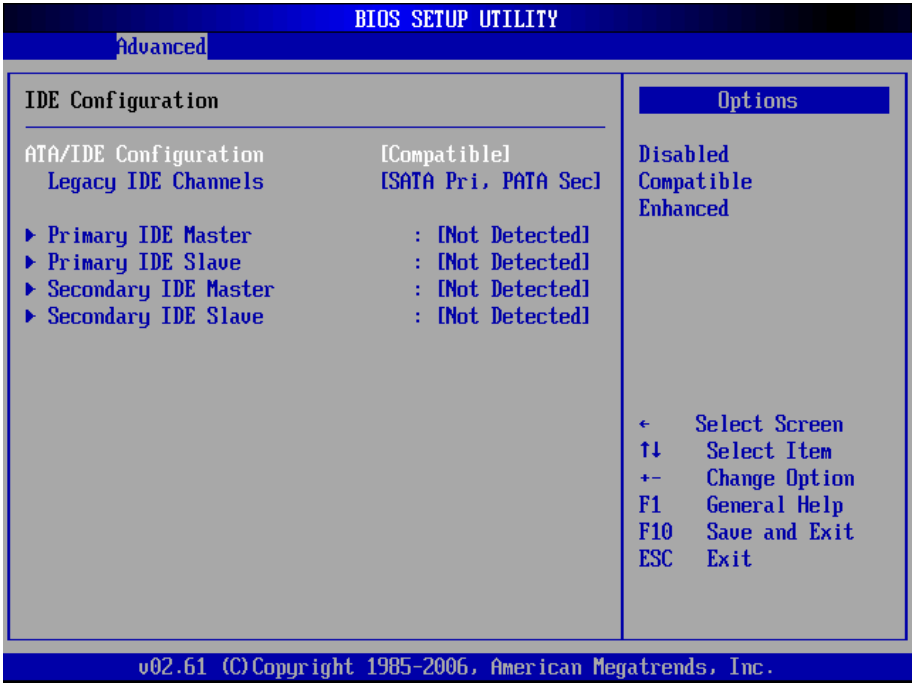


3.2.1 CPU Configuration

The CPU Configuration setup screen varies depending on the installed processor.



3.2.2 IDE Configuration



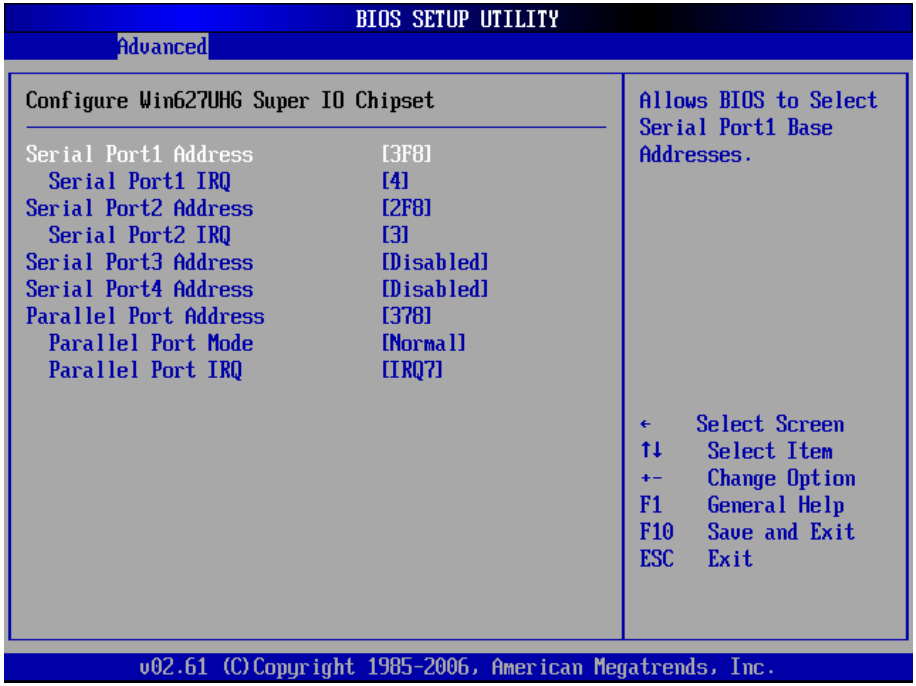
ATA/IDE Configuration

This option is displayed when the ATA/IDE Configuration option is set to Compatible.
Configures PATA and SATA resources for operating systems requiring legacy IDE operation.

Primary/ Secondary IDE Master/ Slave

Select one of the hard disk drives to configure it. Press <Enter> to access its the sub menu.

3.2.3 Super IO Configuration



Serial Port1 /Port2/ Port3/ Port4 Address

Select an address and corresponding interrupt for the first and second serial ports.
The choice:

3F8/IRQ4, 2E8/IRQ3, 3E8/IRQ4, 2F8/IRQ3, Disabled, Auto

Parallel Port Address

Select an address for the parallel port.
The choice:

3BC
378
278
Disabled

Parallel Port Mode

Select an operating mode for the onboard parallel port. Select Normal, Compatible or SPP unless you are certain your hardware and software both support one of the other available modes.

The choice:

SPP
EPP
ECP
ECP + EPP
Normal

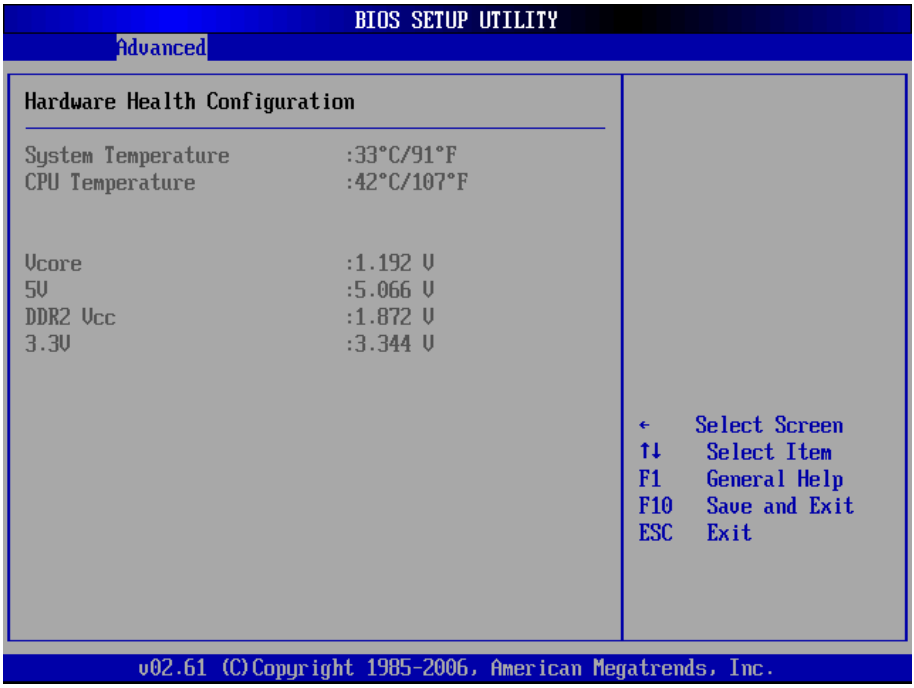
Parallel Port IRQ

Select an interrupt for the parallel port.

The choice:

IRQ5
IRQ7

3.2.4 Hardware Health Configuration



System/ CPU Temperature

Show you the system and CPU temperature..

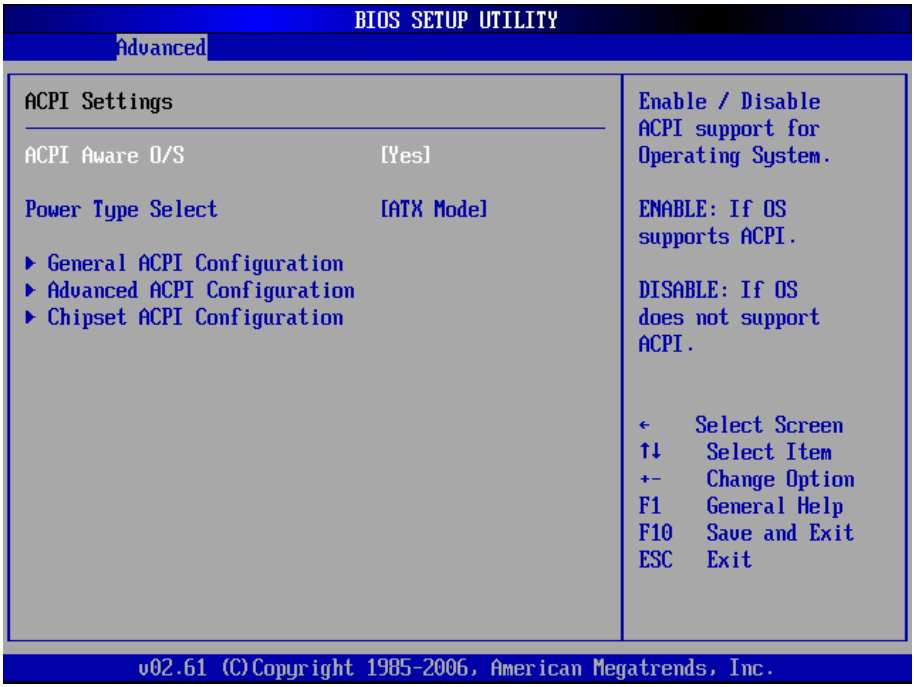
Vcore

Show you the voltage level of CPU (Vcore).

5V / DDR2 Vcc / 3.3V

Show you the voltage level of the +5.0V, DDR2 RAM, and 3.3V.

3.2.5 ACPI Setting



ACPI Aware O/S

This item allows you to enable/disable the Advanced Configuration and Power Management (ACPI)

The Choice: Enabled, Disabled.

Power Type Select

The Choice: ATX Mode (Default), AT Mode.

Power Management/APM

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:
1. HDD Power Down
2. Doze Mode
3. Suspend Mode

Power Button Mode

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has “hang”.

The Choice: Delay 4 Sec, On/Off

Restore on AC Power Loss by IO

This item allows you to select if you want to power on the system after power failure.

Advanced Resume Event Controls

Resume On Ring

An input signal on the serial Ring Indicator (RI) line (in other words an incoming call on the modem) awakens the system from a soft off state.

The Choice: Enabled, Disabled

Resume On PME#

An input signal from a PME on the PCI card awakens the system from a soft off state.

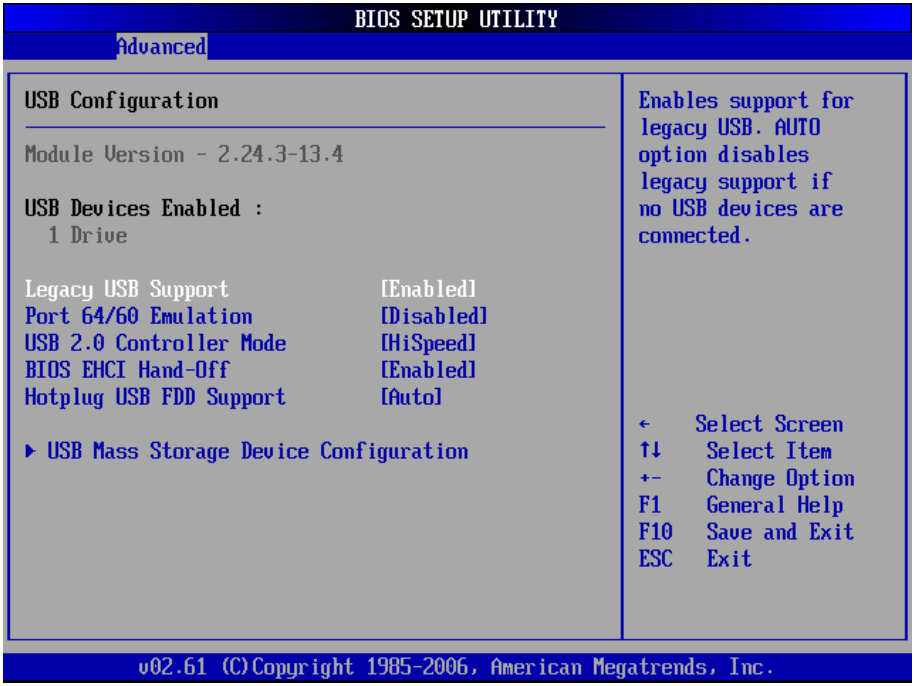
The Choice: Enabled, Disabled

Resume On RTC Alarm

When “Enabled”, you can set the date and time at which the RTC (real-time clock) alarm awakens the system from Suspend mode.

The Choice: Enabled, Disabled

3.2.6 USB Configuration



Legacy USB Support

Enables support for legacy USB. AUTO option disables legacy support if no USB devices are connected.

Port 64/60 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSs.

USB 2.0 Controller Mode

Configures the USB 2.0 controller in High Speed (480Mbps) or Full Speed (12Mbps).

BIOS EHCI Hand-Off

This is a work around for OSs without EHCI hand-Off support. The EHCI ownership change should claim by EHCI driver.

Hotplug USB FDD Support

Allows you to enable or disable the support for a USB floppy disk drive. When set to auto, the system automatically detects the device and enables the support for the device.

USB Mass Storage Device Configuration

Number of seconds POST waits for the USB mass storage device after start unit command.

3.3 Advanced PCI/PnP Settings

Clear NVRAM

Clear NVRAM during System BOOT.

The Choice: Yes, No.

Plug & Play O/S

No: Lets the BIOS configure all the devices in the system.
Yes: lets the operating system configure Plug and Play (PnP) devices not required for BOOT if your system has a Plug and Play operating system.

PCI Latency Timer

Value in units of PCI clocks for PCI device latency timer register.

Allocate IRQ to PCI VGA

Yes: Assigns IRQ to PCI VGA card if card requests IRQ.
No: Does not assign IRQ to PCI VGA card even if card requests an IRQ.

PCI IDE BusMaster

Enabled: BIOS uses PCI busMastering for reading / writing to IDE drives.

Spread Spectrum Function

This item allows you to enable/disable the spread spectrum function.

The Choice: Enabled, Disabled.

IRQ3 - IRQ15

Available: Specified IRQ is available to be used by PCI/PnP devices.
Reserved: Specified IRQ is reserved for use by Legacy ISA devices.

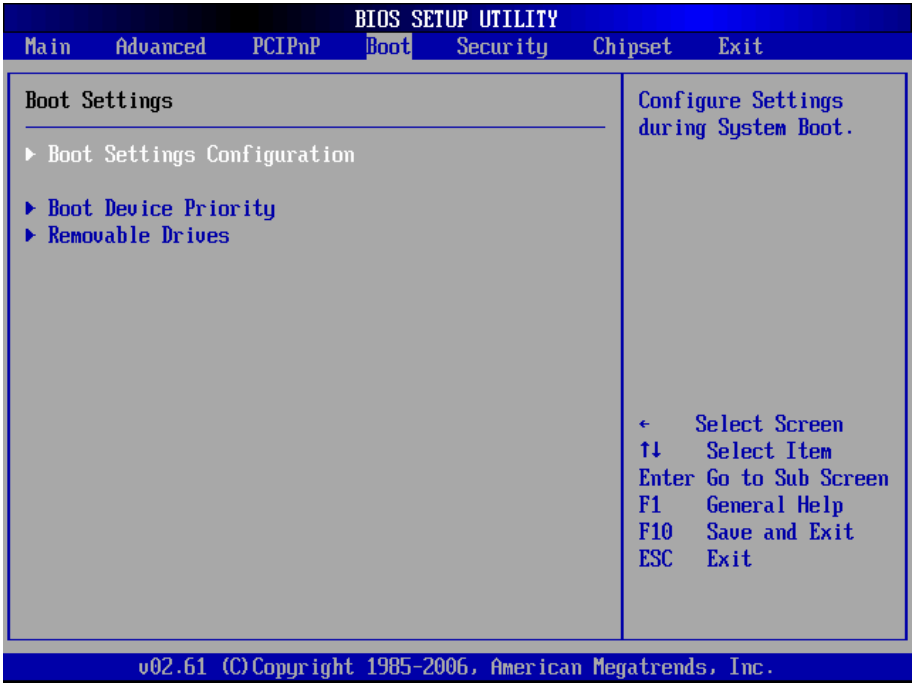
DMA Channel 0 - DMA Channel 7

Available: Specified DMA is available to be used by PCI/PnP devices.
Reserved: Specified DMA is reserved for use by Legacy ISA devices.

Reserved Memory Size

Size of memory block to reserve for legacy ISA devices.

3.4 Boot Settings



Boot Settings Configuration

Press Enter and configure settings during system boot.

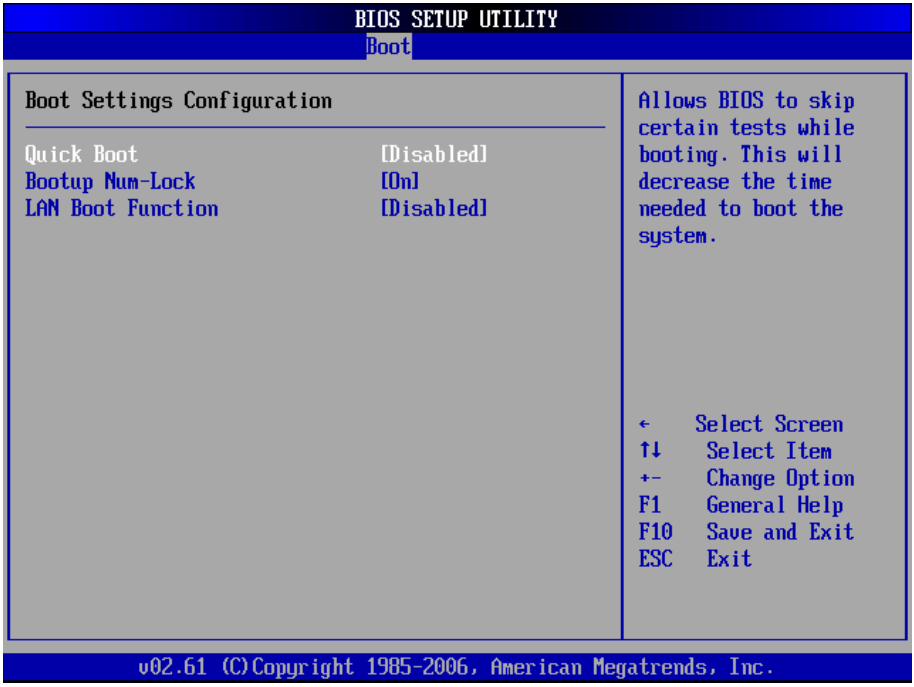
Boot Device Priority

Press Enter and it shows Bootable add-in devices.

Removable Drives

Press Enter and it shows Bootable and Removable drives.

3.4.1 Boot Settings Configuration



Quick Boot

Allows BIOS to skip certain tests while booting. This will decrease the time needed to boot the system.

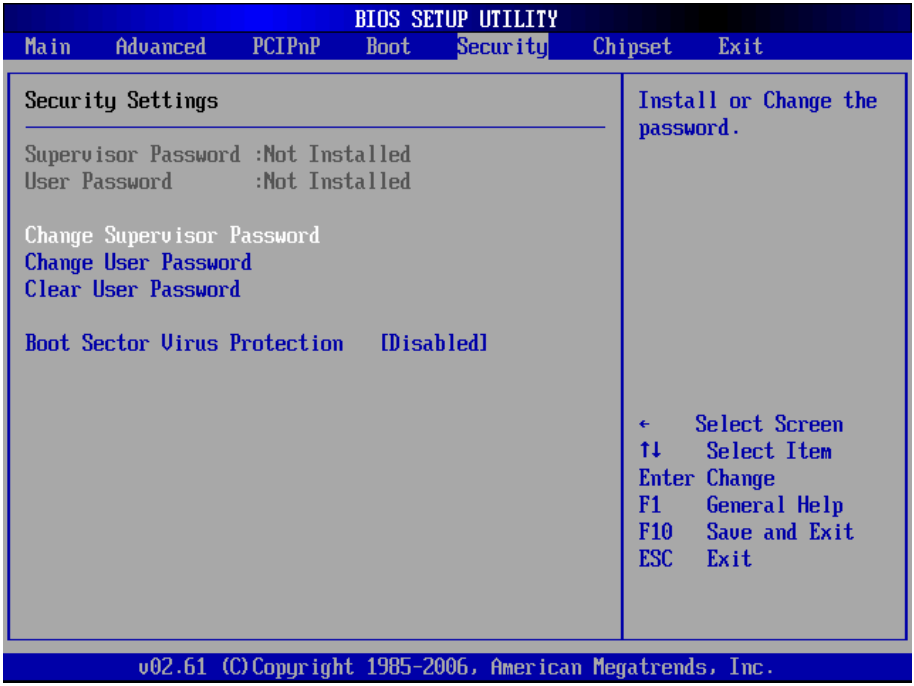
Bootup Num-Lock

Set this value to allow the Number Lock setting to be modified during boot up.

LAN Boot Function

Set this option to LAN add-on Boot ROM function.

3.5 Security



Supervisor Password & User Password

You can set either supervisor or user password, or both of then. The differences between are:

Set ***Supervisor Password***: Can enter and change the options of the setup menus.

Set ***User Password***: Just can only enter but do not have the right to change the options of the setup menus. When you select this function, the following message will appear at the center of the screen to assist you in creating a password.

ENTER PASSWORD:

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <ESC> to abort the selection and not enter a password.

To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration.

Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer.

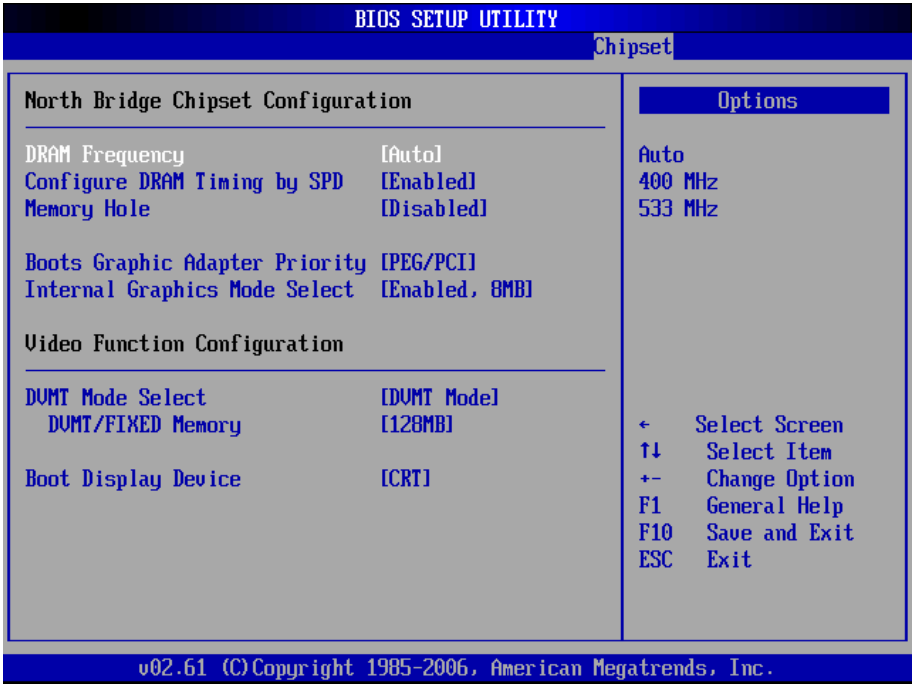
You determine when the password is required within the BIOS Features Setup Menu and its Security option. If the Security option is set to “System”, the password will be required both at boot and at entry to Setup. If set to “Setup”, prompting only occurs when trying to enter Setup.

Boot Sector Virus Protection

Enable/Disable Boot Sector Virus Protection.

3.6 Advanced Chipset Settings

3.6.1 North Bridge Chipset Configuration



DRAM Frequency

The item allows you to set the DRAM frequency.

Configure DRAM Timing by SPD

Select the operating system that is selecting SRAM timing, so select SPD for setting SDRAM timing by SPD.

The Choice: Enable, Disable

Memory Hole

The Choice: Enable, Disable

Boots Graphic Adapter Priority

Select which graphics controller to use as the primary boot device.

Internal Graphic Mode Select

Select the amount of system memory used by the Internal graphics device.

VIdeo Function Configuration

DVMT Mode Select

This item allows you to configure the DVMT Mode.

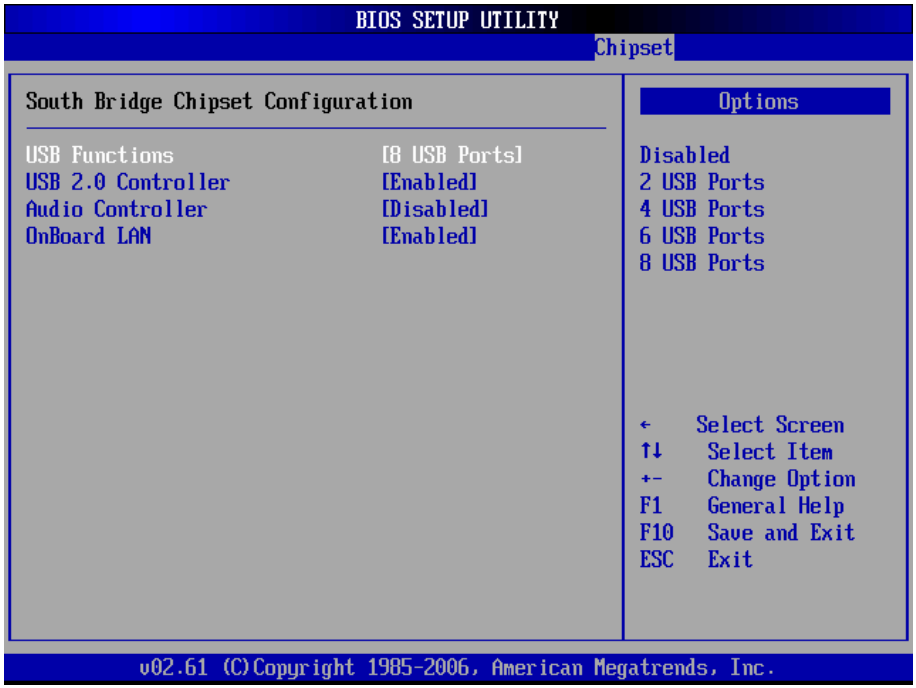
The Choice: Fixed , DVMT

DVMT/FIXED Memory

This item allows you to configure the DVMT memory size.

The Choice: 128MB, 256MB.

3.6.2 South Bridge Chipset Configuration



USB Funtion

This item allows you to active USB ports.

The Choice:

Disabled
2 USB Ports
4 USB Ports
6 USB Ports
8 USB Ports

USB 2.0 Controller

Select “Enabled” if your system contains a Universal Serial Bus 2.0 (USB 2.0) controller and you have USB peripherals.

The Choice: Enabled, Disabled.

Audio Controller

This item allows you to select the chipset family to support AC97/ High Definition Audio Controller. If an AC97 Aduio daughter board is connected, select AC97 Audio Only. If an HD Audio daughter board is connected, select Azalia in this field.

The Choice: Disabled (Default), AC97 Audio Only, Azalia.

OnBoard LAN

The Choice: Enabled (Default), Disabled.

3.7 Exit Options

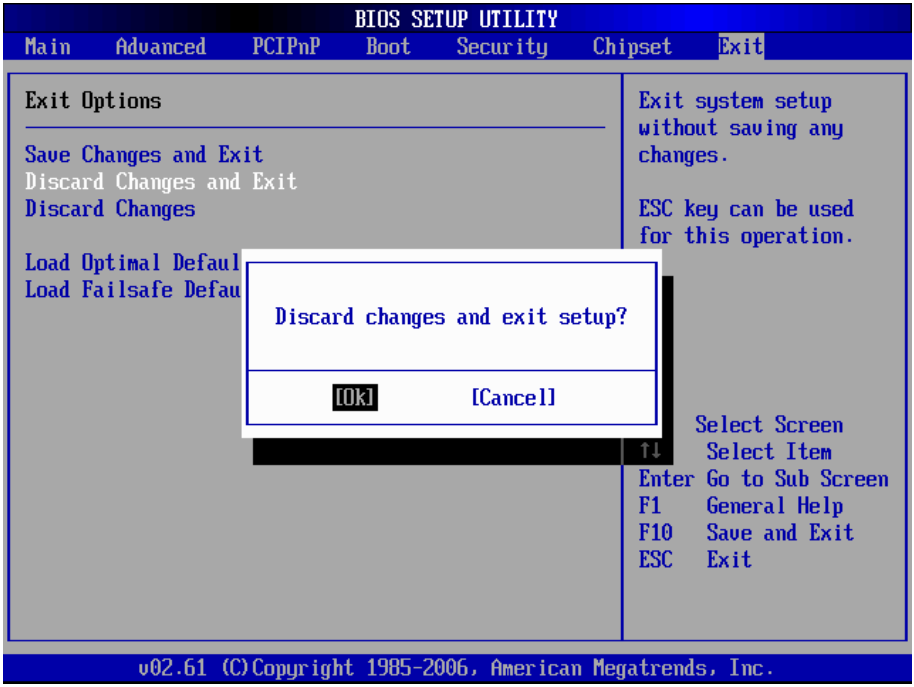
Save Changes and Exit

Pressing <Enter> on this item asks for confirmation:

Save configuration changes and exit setup?

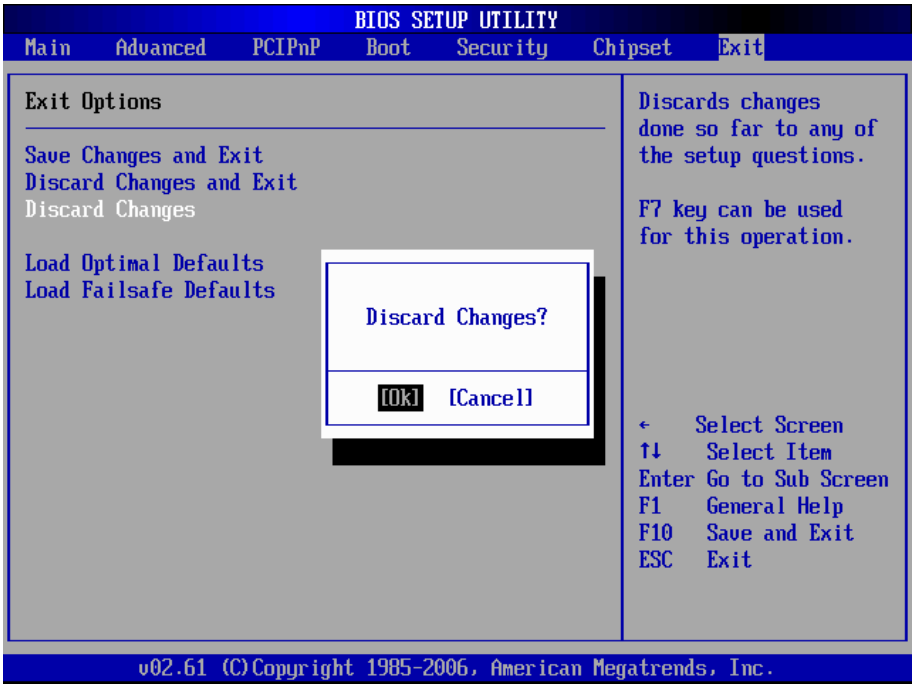
Pressing <OK> stores the selection made in the menus in CMOS - a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again.

Discard Changes and Exit



Exit system setup without saving any changes.
<ESC> key can be used for this operation.

Discard Changes



Discards changes done so far to any of the setup questions.
<F7> can be used for this operation.

Load Optimal Defaults

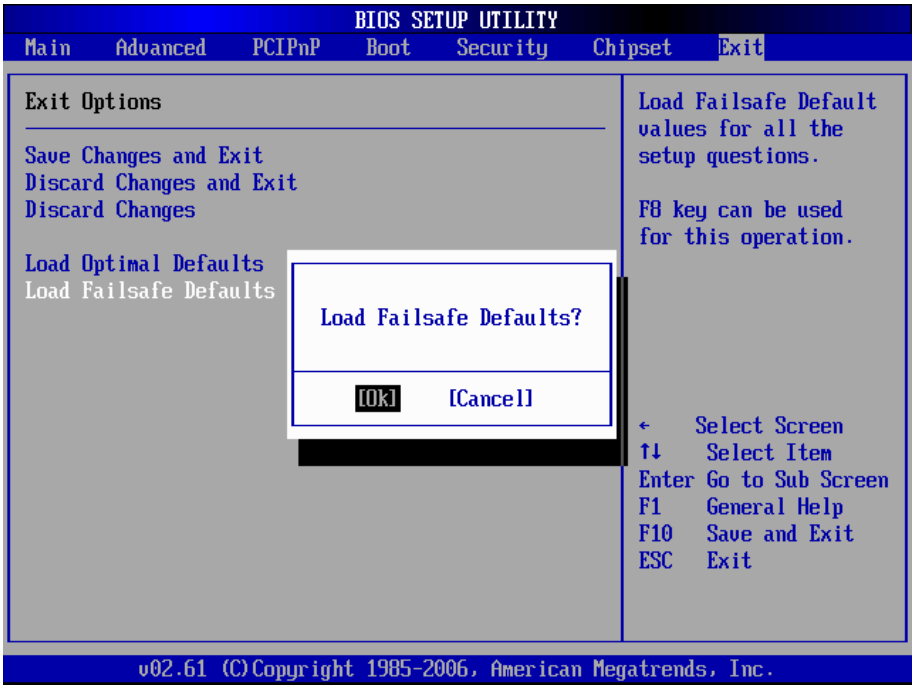
When you press <Enter> on this item you get a confirmation dialog box with a message:

Load Optimal Defaults?
[OK] [Cancel]

Pressing [OK] loads the BIOS Optimal Default values for all the setup questions.

<F9> key can be used for this operation.

Load Failsafe Defaults



When you press <Enter> on this item you get a confirmation dialog box with a message:

Load Failsafe Defaults?
[OK] [Cancel]

Pressing [OK] loads the BIOS Failsafe Default values for all the setup questions.

<F8> key can be used for this operation.

3.8 Beep Sound codes list

3.8.1 Boot Block Beep codes

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

3.8.2 POST BIOS Beep codes

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

3.8.3 Troubleshooting POST BIOS Beep codes

Number of Beeps	Description
1, 2 or 3	Reseat the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond all hope, eliminate the possibility of interference by a malfunctioning add-in card. Remove all expansion cards except the video adapter. • If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support. • If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem
8	If the system video adapter is an add-in card, replace or reseat the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

3.9 AMI BIOS Checkpoints

3.9.1 Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS *(Note)*:

Checkpoint	Description
Before D0	If boot block debugger is enabled, CPU cache-as-RAM functionality is enabled at this point. Stack will be enabled from this point.
D0	Early Boot Strap Processo (BSP) initialization like microcode update, frequency and other CPU cirtical initialization. Early chipset initialization is done.
D1	Early super I/O initialization is done including RTC and keyboard controller. Serial port is enabled at this point if needed for debugging. NMI is deisabled. Perfrom keyboard controller BAT test. Save power-on CPUID value in scretch CMOS. Go to flat mode with 4GB limit and GA20 enabled.
D2	Verify the boot block checksum. System will hang here if checksum is bad.
D3	Disable CACHE before memory detection. Execute full memory sizing module. If memory sizing module not executed, start memory refresh and do memory sizing in Boot block code. Do additional chipset initialization. Re-enabled CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM. Copies compressed boot block code to memory in right segments. Copies BIOS from ROM to RAM for faster access. Perfroms main BIOS checksum and updates recovery status accordingly.

D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. If BIOS recovery is necessary, control flows tocheckpoint E0. Seed *Bootblock Recovery Code Checkpoints* section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether in memory.
D8	The Tuntime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POS (ExecutePOSTKernel). See *POST Code Checkpoints* section of document for more information.
DC	System is saking from ACPI S3 state.
E1 - E8 EC - EE	OEM memory detection / configuration error. This range is reserved for chipset vendors & system manufacturers. The error associated with this value may be different from one platform to be next.

3.9.2 Bootblock Recovery Code Checkpoints

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS *(Note)*:

Checkpoint	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA controller is initialized. 8259 interrupt controller is initialized. L2 cache is enabled.
E9	Set up floppy controller and data. Attempt to red from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
F4	The recovery file size does not equal the found flash part size.

FC	Erase the flash part.
FD	Program the flash part.
FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

3.9.3 POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS *(Note)*:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system.
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
07	Fixes CPU POST interface calling pointer.
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
C0	Early CPU Init Start -- Disable Cache - Init Local APIC
C1	Set up boot strap processor Information
C2	Set up boot strap processor for POST
C5	Enumerate and set up application processors
C6	Re-enable cache for boot strap processor

C7	Early CPU Init Exit
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.
13	Early POST initialization of chipset registers.
20	Relocate System Management Interrupt vector for all CPU in the system.
24	Uncompress and initialize any platform specific BIOS modules. GPNV is initialized at this checkpoint.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.

38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information. USB controllers are initialized at this point.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory. Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7C	Generate and write contents of ESCD in NVRam.
84	Log errors encountered during POST.
85	Display errors to theuser and gets the user response for error.
87	Execute BIOS setup if needed / requested. Check boot password if installed.
8C	Late POST initialization of chipset registers.
8D	Build ACPI tables (if ACPI is supported)
8E	Program the peripheral parameters. Enable/Disalbe NMI as selected.
90	Initialization of system management interrupt by invoking all handlers.
A1	Lian-up work needed before booting to OS.

A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module. Display boot option popup menu.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A9	Wait for userinput at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector.
AB	Prepare BBS for Int 19 boot. Init MP tables.
AC	End of POST initialization of chipset registers. De-initializes the ADM module.
B1	Save system context for ACPI. Prepare CPU for OS boot including final MTRR values.
00	Passes control to OS Loader (typically INT19h).

3.9.4 DIM Code Checkpoints

The Device Initialization Manager (DIM) gets control at various times during BIOS POST to initialize different system buses. The following table describes the main checkpoints where the DIM module is accessed *(Note)*:

Checkpoint	Description
2A	Initialize different buses and perform the following functions: Reset, Detect, and Disable (function 0); Static Device Initialization (function); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices, and PnP ISA cards. It also assigns PCI bus numbers. Function 1 initializes all static devices that include manual configured onboard peripherals, memory and I/O decode windows in PCI-PCI bridges, and noncompliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI, or AGP video devices.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all onboard peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

While control is in the different functions, additional checkpoints are output to port 80h as a word value to identify the routines under execution. The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two fields. The details of the high byte of these checkpoints are as follows:

HIGH BYTE XY

The upper nibble “X” indicates the function number that is being executed. “X” can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
2 = func#2, output device initialization on the BUS concerned.
3 = func#3, input device initialization on the BUS concerned.
4 = func#4, IPL device initialization on the BUS concerned.
5 = func#5, general device initialization on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM initialization for all BUSes.
8 = func#8, BBS ROM initialization for all BUSes.

The lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = On-board System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

3.9.5 ACPI Runtime Checkpoints

ACPI checkpoints are displayed when an ACPI capable operating system either enters or leaves a sleep state. The following table describes the type of checkpoints that may occur during ACPI sleep or wake events *(Note)*:

Checkpoint	Description
AC	First ASL check point. Indicates the system is running in ACPI mode.
AA	System is running in APIC mode.
01, 02, 03, 04, 05	Entering sleep state S1, S2, S3, S4, or S5.
10, 20, 30, 40, 50	Waking from sleep state S1, S2, S3, S4, or S5.

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Chapter 4

Appendix

4.1 I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device.
The following table lists the I/O port addresses used.

Address	Device Description
00000000 - 0000000F	DMA Controller
00000080 - 0000009F	DMA Controller
000000C0 - 000000DF	DMA Controller
00000020 - 00000021	Programmable Interrupt Controller
000000A0 - 000000A1	Programmable Interrupt Controller
00000040 - 00000043	System Timer
00000044 - 00000047	System Timer
00000060 - 00000064	Keyboard Controller
00000070 - 00000073	System CMOS/Real Time Clock
000000F0 - 000000FF	Math Co-processor
00000170 - 00000177	Secondary IDE
000001F0 - 000001F7	Primary IDE
00000274 - 00000277	ISAPNP Read Data Port
00000279, 00000A79	ISAPNP Configuration
000002F8 - 000002FF	Communications Port (COM2, If use)
00000376 - 00000376	Secondary IDE
000003B0 - 000003BF	MDA/MGA
000003C0 - 000003CF	EGA/VGA
000003D4 - 000003D9	CGA Analog RGB register
000003F0 - 000003F7	Floppy Diskette
000003F6 - 000003F6	Primary IDE
000003F8 - 000003FF	Communications Port (COM1, If use)
00000400 - 0000041F	South Bridge SMB
00000480 - 000004BF	South Bridge GPIO
00000800 - 0000087F	ACPI

00000A00 - 00000A07	PME
00000A10 - 00000A17	Hardware Monitor
0000CF8	PCI Configuration address
00000CFC	PCI Configuration Data

4.2 Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System Timer
IRQ 1	Keyboard Controller
IRQ 2	VGA and Link to Secondary PIC
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	PCI Device
IRQ 6	Standard Floppy Disk Controller
IRQ 7	Parallel Port
IRQ 8	System CMOS/real time clock
IRQ 9	Microsoft ACPI-Compliant System
IRQ 10	PCI Device
IRQ 11	PCI Device
IRQ 12	PS/2 Compatible Mouse
IRQ 13	FPU Exception
IRQ 14	IDE Controller
IRQ 15	IDE Controller

4.3 BIOS memory mapping

Address	Device Description
00000h - 9FFFFh	DOS Kernel Area
A0000h, BFFFFh	EGA and VGA Video Buffer (128KB)
C00000h - CFFFFh	EGA/VGA ROM
D0000h - DFFFFh	Adaptor ROM
E00000h - FFFFFh	System BIOS

4.4 Watchdog Timer (WDT) Setting

WDT is widely used for industry application to monitoring the activity of CPU. Application software depends on its requirement to trigger WDT with adequate timer setting. Before WDT time out, the functional normal system will reload the WDT. The WDT never time out for a normal system. Then, WDT will time out and reset the system automatically to avoid abnormal operation.

This board supports 255 levels watchdog timer by software programming. Below are the source codes written in assembly & C, please take them for WDT application examples.

Assembly Code

```
mov     ax,2eh
mov     dx,ax
mov     ax,87h
out     dx,al
out     dx,al           ; initial IO port twice

mov     ax,2eh
mov     dx,ax
mov     al,07h          ; point to logical device selector
out     dx,al
inc     dx
mov     al,08h
out     dx,al           ; select logical device 8

mov     ax,2eh
mov     dx,ax
```

```
mov     al,30h          ; select CR30
out     dx,al
inc     dx
mov     al,01h
out     dx,al           ; update CR30 to 01h, WDTO enable

mov     ax,2eh
mov     dx,ax
mov     al,0f5h         ; select CRF5 to set timer unit
out     dx,al
inc     dx
mov     al,00h
out     dx,al           ; update CRF5 bit3, 0:sec; 1:Min.

mov     ax,2eh
mov     dx,ax
mov     al,0f6h         ; select CRF6
out     dx,al
inc     dx
mov     al,05h
out     dx,al           ; update CRF6 to 05h (5 sec)

mov     ax,2eh
mov     dx,ax
mov     ax,0aah
out     dx,al           ;stop program W83627UHG, Exit
```

C Language Code

```
/*-----     Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*-----     routing, sub-routing -----*/

void main()
{
          outportb(0x2e, 0x87);       /* initial IO port twice */
          outportb(0x2e, 0x87);

          outportb(0x2e, 0x07);       /* point to logical device selector */
          outportb(0x2e+1, 0x08);     /* select logical device 8 */
          outportb(0x2e, 0x30);       /* select CR30 */
          outportb(0x2e+1, 0x01);     /* update CR30 to 01h, WDTO enable*/
          outportb(0x2e, 0xf5);       /* select CRF5 to set timer unit */
          outportb(0x2e+1, 0x00);     /* update CRF5 bit3, 0:sec; 1:Min. */
          outportb(0x2e, 0xF6);       /* select CRF6 */
          outportb(0x2e+1, 0x05);     /* update CRF6 to 05h (5 sec) */

          outportb(0x2e, 0xAA);       /* stop program W83627UHG, Exit */

}
```

4.5 Digital I/O Setting

Below are the source codes written in assembly & C, please take them for Digital I/O application examples. The default I/O address is 6Eh.

Assembly Code

```
mov     ax,2eh
mov     dx,ax
mov     ax,87h
out     dx,al
out     dx,al           ; initial IO port twice

mov     ax,2eh
mov     dx,ax
mov     al,07h          ; point to logical device selector
out     dx,al
inc     dx
mov     al,08h
out     dx,al           ; select logical device 8

mov     ax,2eh
mov     dx,ax
mov     al,30h          ; select CR30
out     dx,al
inc     dx
mov     al,02h
out     dx,al           ; set bit1=1, GPIO port 5 active

mov     ax,2eh
mov     dx,ax
mov     al,0e0h         ; elect CRE0, GP I/O select
out     dx,al
inc     dx
mov     al,00h
out     dx,al           ; bit7~bit0 0:output  1:input

mov     ax,2eh
mov     dx,ax
mov     al,0e1h         ; select CRF1, Data Register
out     dx,al
inc     dx
mov     al,0ffh
```

```
out     dx,al           ; set all GPIO pin output 1

mov     ax,2eh
mov     dx,ax
mov     al,0e1h         ; select CRF1, Data Register
out     dx,al
inc     dx
mov     al,000h
out     dx,al           ; set all GPIO pin output 0

mov     ax,2eh
mov     dx,ax
mov     ax,0aah
out     dx,al           ;stop program W83627UHG, Exit
```

C Language Code

```
/*-----     Include Header Area -----*/
#include "math.h"
#include "stdio.h"
#include "dos.h"

/*-----     routing, sub-routing -----*/

void main()

{
          outportb(0x2e, 0x87);
          /* initial IO port twice */
          outportb(0x2e, 0x87);

          outportb(0x2e, 0x07);       /* point to logical device */
          outportb(0x2e+1, 0x08);     /* select logical device 8 */

          outportb(0x2e, 0x30);       /* select CR30 */
          outportb(0x2e+1, 0x02);     /* set bit1=1, GPIO port 5 active */

          outportb(0x2e, 0xe0);       /* select CRE0, GP I/O select */
          outportb(0x2e+1, 0x00);     /* bit7~bit0 0:output  1:input */

          outportb(0x2e, 0xe1);       /* select CRE1, Data Register */
          outportb(0x2e+1, 0xff);     /* set all GPIO pin output 1 */

          outportb(0x2e, 0xe1);       /* select CRE1, Data Register */
          outportb(0x2e+1, 0x00);     /* set all GPIO pin output 0 */

          outportb(0x2e, 0xAA);       /* stop program W83627UHG, Exit */

}
```

Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support you for your products, projects and business.

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